FAST GATE TURN—OFF THYRISTORS

Thyristors in TO-238AA envelopes with electrically isolated metal baseplates capable of being turned both on and off via the gate. They are suitable for use in high-frequency inverters, power supplies, motor control etc. The devices have no reverse blocking capability. For reverse blocking operation use with a series diode, for reverse conducting operation use with an anti-parallel diode.

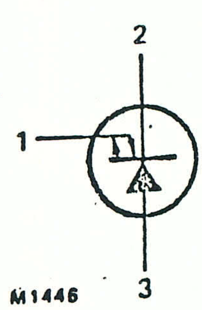
QUICK REFERENCE DATA

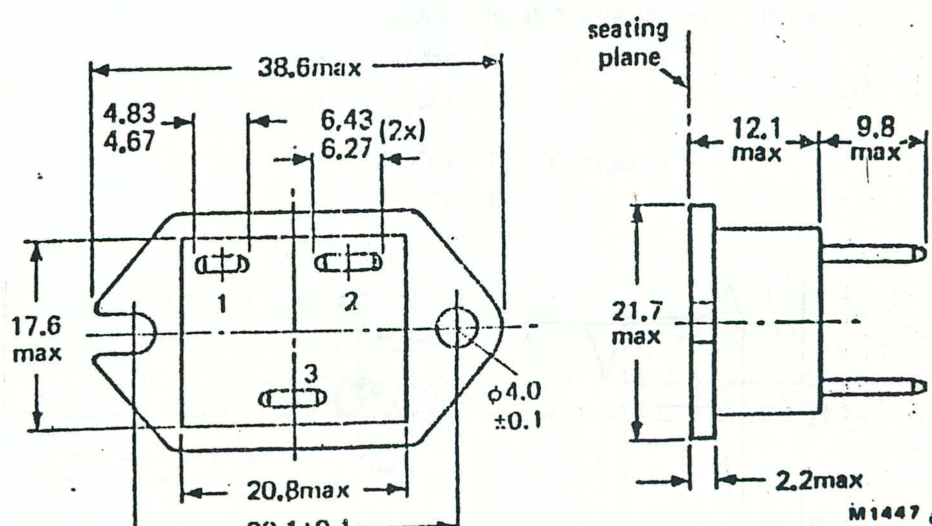
			BTV60—850R	1000R	1200R	
Repetitive peak off-state voltage	V_{DRM}	max.	850	1000	1200	V
Non-repetitive peak on-state current	I_{TSM}	max.		150		A
Controllable anode current	I_{TCRM}	max.		120		A
Average on-state current	$I_{T(AV)}$	max.		25		A
Fall time	t_f	<		300		ns

MECHANICAL DATA

Dimensions in mm

Fig.1 TO-238AA





Pin 1 = gate (AMP 187 series)
2 = cathode (AMP 250 series)
3 = anode (AMP 250 series)
Baseplate is electrically isolated.

blue binder, tab 9

RATINGS

Limiting values in accordance with the absolute Maximum System (IEC134)

Anode to cathode			BTV60–850R	1000R	1200R	
Transient off-state voltage	V_{DSM}	max.	1000	1100	1300	V*
Repetitive peak off-state voltage	V_{DRM}	max.	850	1000	1200	V*
Working off-state voltage	V_{DW}	max.	600	800	1000	V*
Continuous off-state voltage	V_D	max.	500	650	750	V*

Average on-state current (averaged over any 20 ms period) up to T_{mb} = 70 °C	$I_{T(AV)}$	max.	25	A
Controllable anode current	I_{TCRM}	max.	120	A
Non-repetitive peak on-state current t = 10 ms; half-sinewave; T_j = 120 °C prior to surge	I_{TSM}	max.	150	A
I^2t for fusing; t = 10 ms	I^2t	max.	112	A^2s
Total power dissipation up to T_{mb} = 25 °C	P_{tot}	max.	120	W
Gate to cathode				
Repetitive peak on-state current T_j = 120 °C prior to surge				
gate-cathode forward; t = 10 ms; half-sinewave	I_{GFM}	max.	35	A
gate-cathode reverse; t = 20 µs	I_{GRM}	max.	50	A
Average power dissipation (averaged over any 20 ms period)	$P_{G(AV)}$	max.	10	W
Temperatures				
Storage temperature	T_{stg}		−40 to +150	°C
Operating junction temperature	T_j	max.	120	°C

ISOLATION**

R.M.S. isolation voltage	V_{isol}	min.	2500	V

THERMAL RESISTANCE

From mounting base to heatsink; with heatsink compound	$R_{th\ mb\text{-}h}$	=	0.3	K/W
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	0.8	K/W

* Measured with gate-cathode connected together.
** From baseplate to all terminals strapped together.

CHARACTERISTICS

Anode to cathode

On-state voltage $I_T = 20$ A; $I_G = 0.5$ A; $T_j = 120$ °C	V_T	<	2.2	V*
Rate of rise of off-state voltage that will not trigger any off-state device; exponential method $V_D = 2/3\ V_{Dmax}$; $V_{GR} = 5$ V; $T_j = 120$ °C	dV_D/dt	<	10	kV/
Rate of rise of off-state voltage that will not trigger any device following conduction, linear method $I_T = 60$ A; $V_D = V_{DRMmax}$; $V_{GR} = 10$ V; $T_j = 120$ °C	dV_D/dt	<	1.0	kV/
Off-state current $V_D = V_{Dmax}$; $T_j = 120$ °C	I_D	<	5.0	mA
Latching current; $T_j = 25$ °C	I_L	typ.	5.0	A**

Gate to cathode

Voltage that will trigger all devices $V_D = 12$ V; $T_j = 25$ °C	V_{GT}	>	1.5	V
Current that will trigger all devices $V_D = 12$ V; $T_j = 25$ °C	I_{GT}	>	500	mA
Minimum reverse breakdown voltage $I_{GR} = 1.0$ mA	$V_{(BR)GR}$	>	10	V

Switching characteristics (resistive load)

Turn-on when switched to $I_T = 50$ A from $V_D = 250$ V with $I_{GF} = 2.5$ A; $T_j = 25$ °C				
delay time	t_d	<	0.5	µs
rise time	t_r	<	2.0	µs

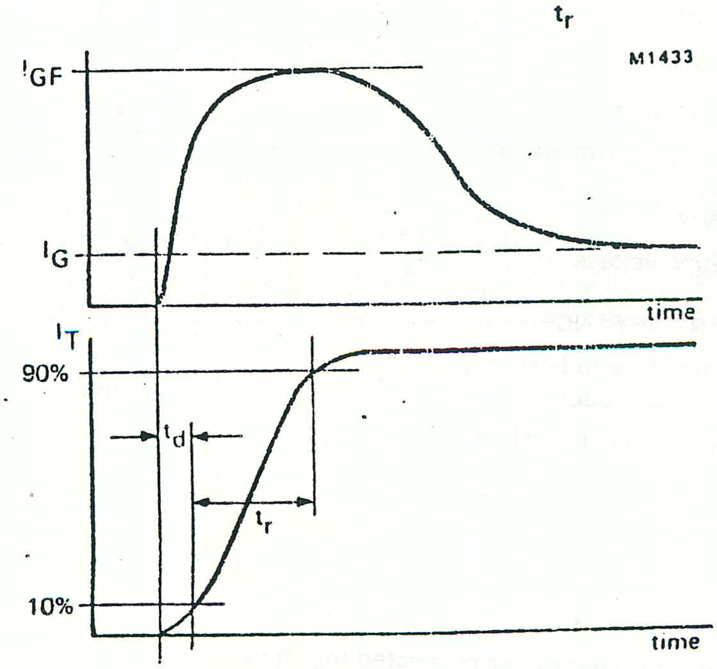


Fig.2 Waveforms.

*Measured under pulse conditions to avoid excessive dissipation.

**Below latching level the device behaves like a transistor with a gain dependent on current.

Switching characteristics (inductive load)

Turn-off when switched from I_T = 50 A to $V_D = V_{Dmax}$;
V_{GR} = 10 V; $L_G \leqslant 0.5\ \mu H$; $L_S \leqslant 0.25\ \mu H$; T_j = 25 °C

storage time	t_s	<	1.0
fall time	t_f	<	0.3
peak reverse gate current	I_{GR}	<	25

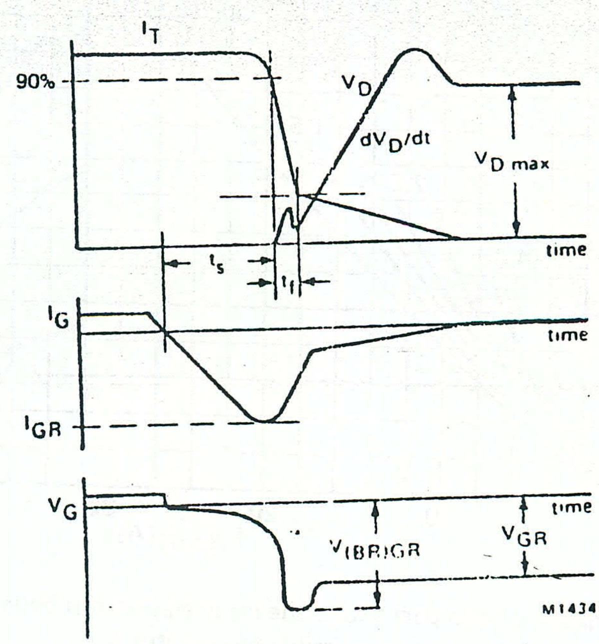


Fig.3 Wave

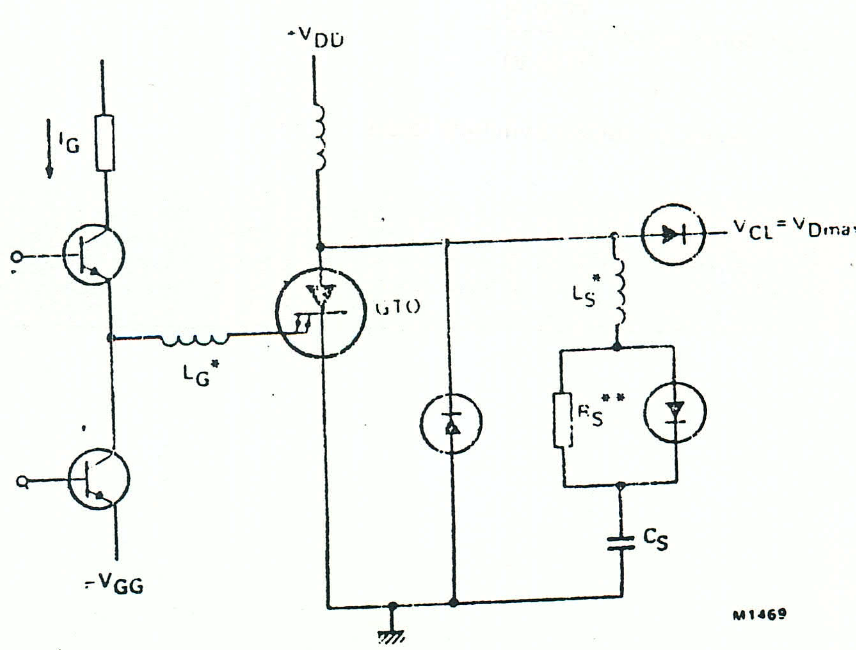


Fig.4 Indu
load test

*Indicates stray series inductance only.
**Minimum permissible GTO on-time (µs) = R_S (Ω) x C_S (µF) x 5.

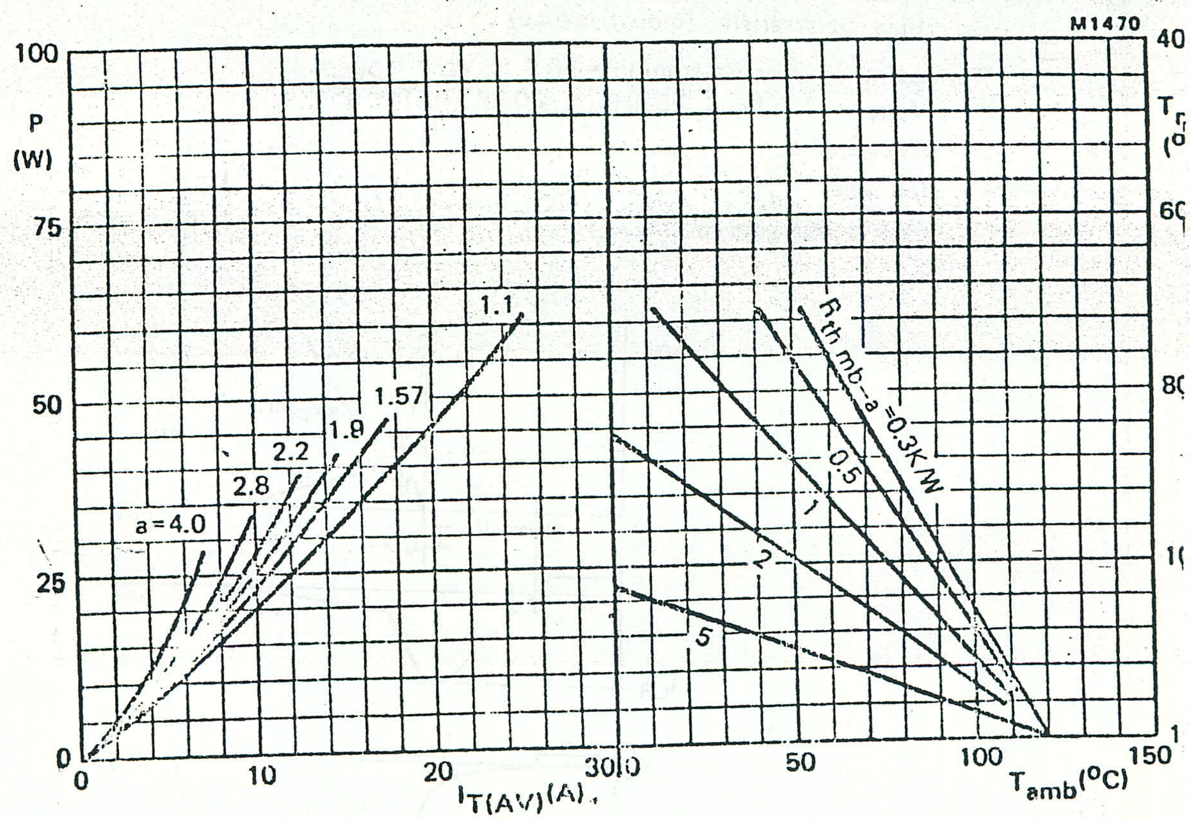


Fig.5 The right hand part shows the interrelationship between the power (derived from the left-hand part) and the maximum permissible temperatures.

$$a = \text{form factor} = \frac{I_{T(RMS)}}{I_{T(AV)}}$$

P = power excluding switching losses.

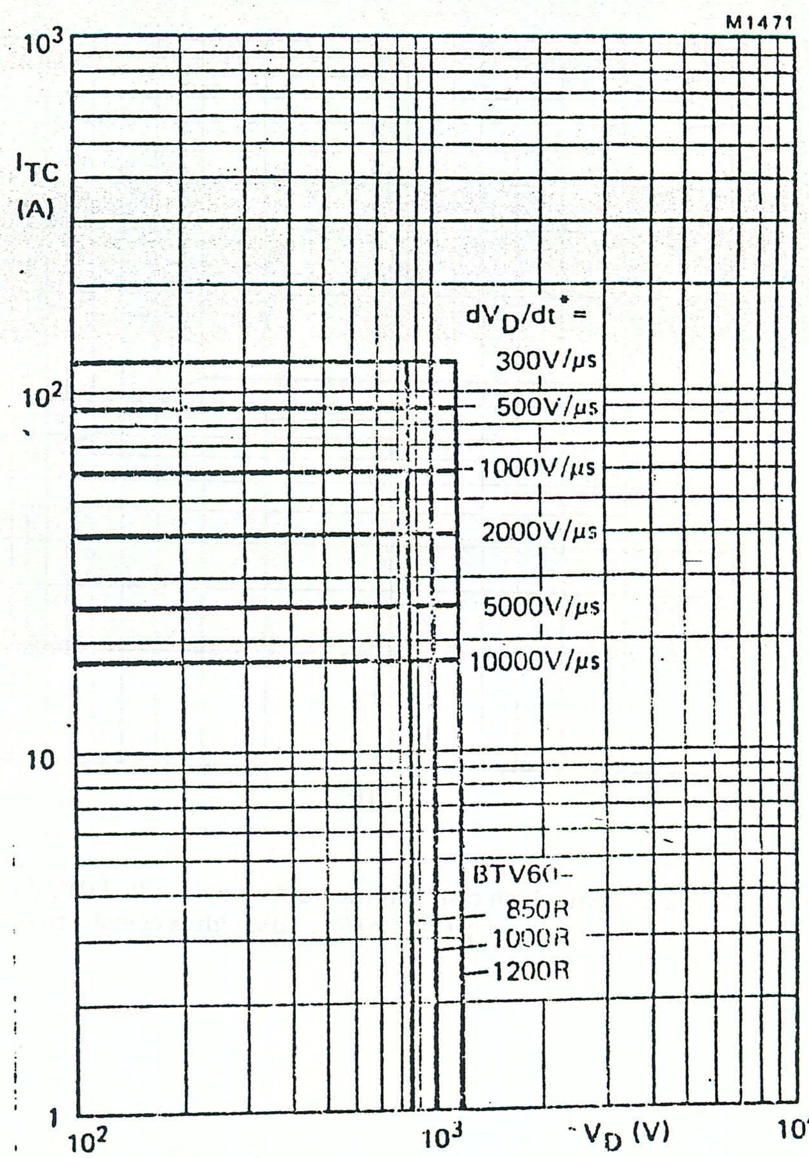


Fig.6 Anode current which can be turned off versus anode voltage; inductive load; V_{GR} = 10 V; $L_G \leq 0.5\ \mu H$; $L_S \leq 0.25\ \mu H$; T_j = 120 °C.
*dV_D/dt is calculated from I_T/C_S.

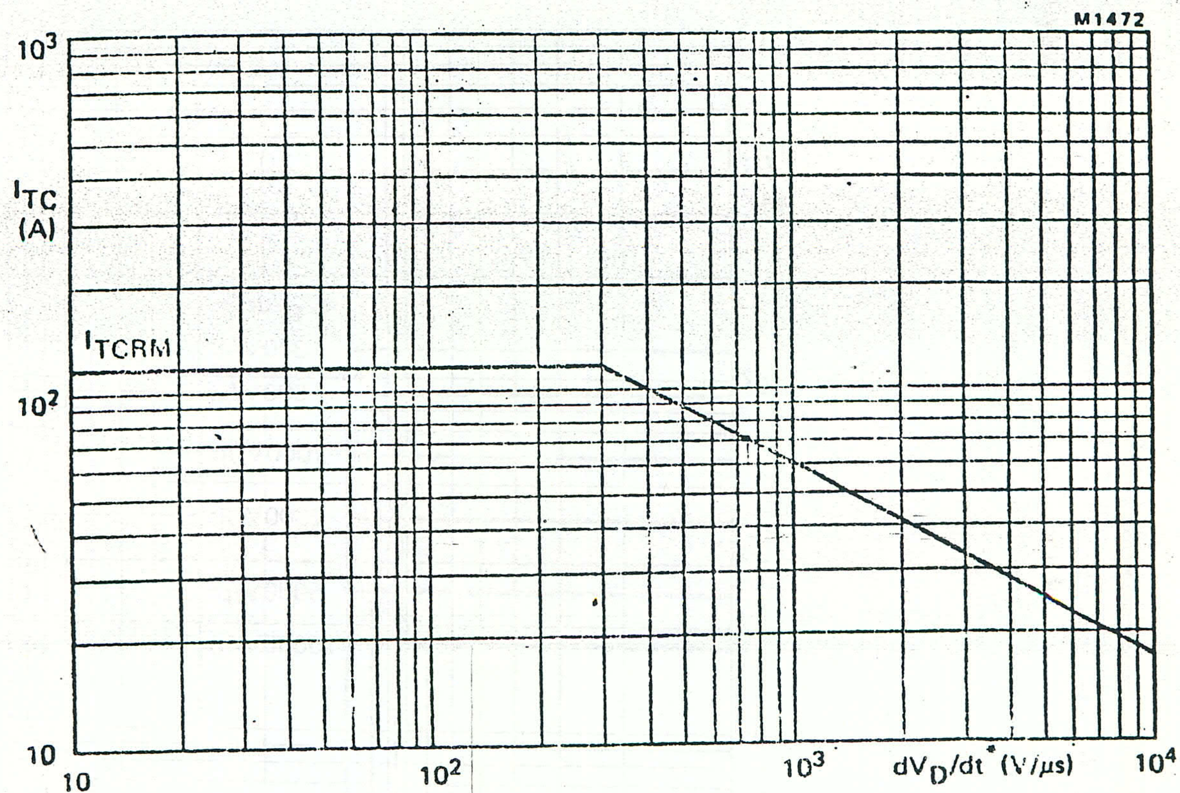


Fig.7 Anode current which can be turned off versus applied dV_D/dt^*: inductive load; V_{GR} = 10 V; $L_G \leq 0.5$ µH; $L_S \leq 0.25$ µH; T_j = 120 °C. *dV_D/dt is calculated from I_T/C_S.

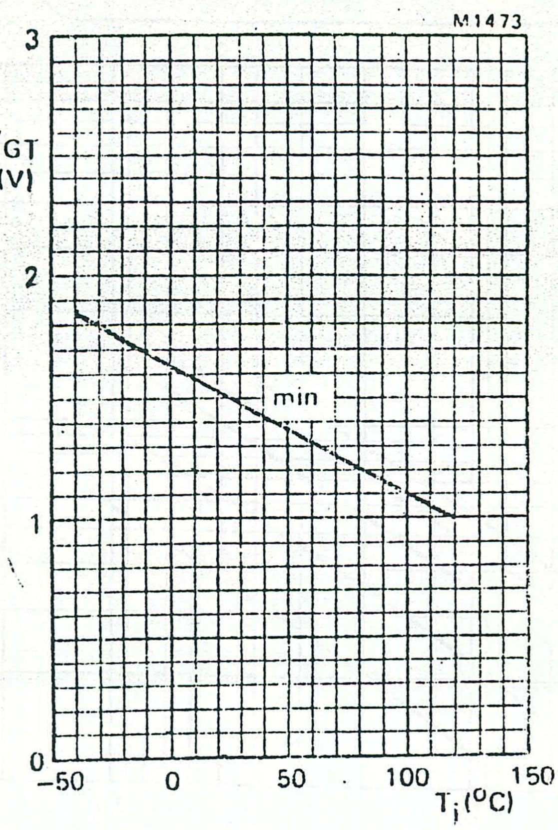


Fig.8 Minimum gate voltage that will trigger all devices as a function of junction temperature; V_D = 12 V.

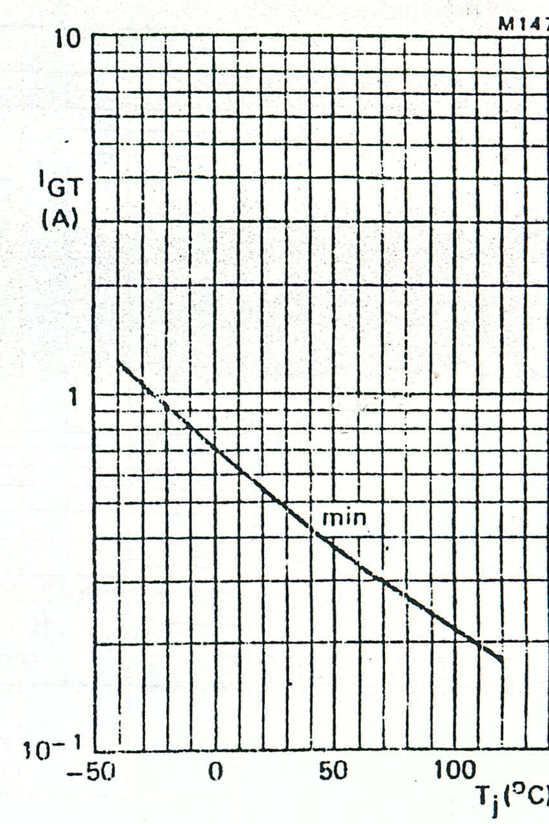


Fig.9 Minimum gate current that will trigger all devices as a function of junction temperature; V_D = 12 V.

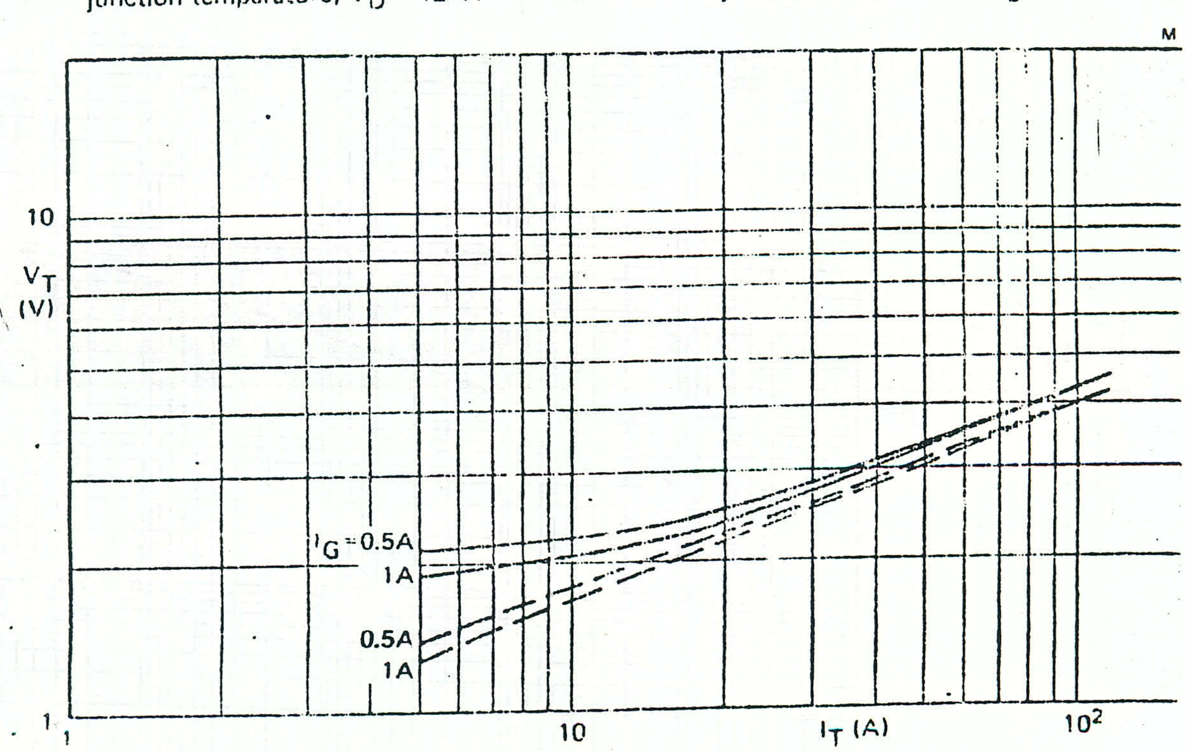


Fig.10 Maximum V_T versus I_T; —— T_j = 25 °C; – – – – T_j = 120 °C.

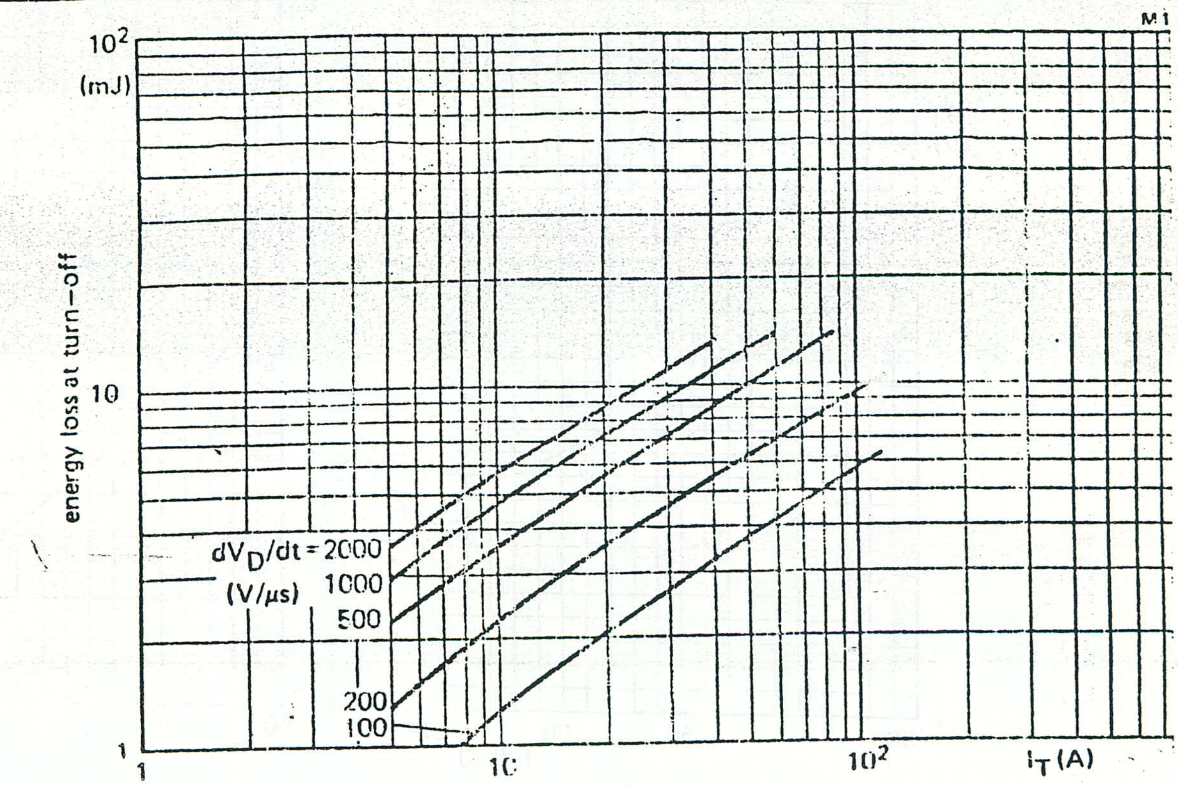


Fig.11 Maximum energy loss at turn-off (per cycle) as a function of anode current and app dV_D/dt (calculated from I_T/C_S); dV_D/dt linear up to V_{Dmax} = 600 V; V_{GR} = 10 V; I_G = $L_G \leq 0.5$ μH; $L_S \leq 0.25$ μH; T_j = 120 °C

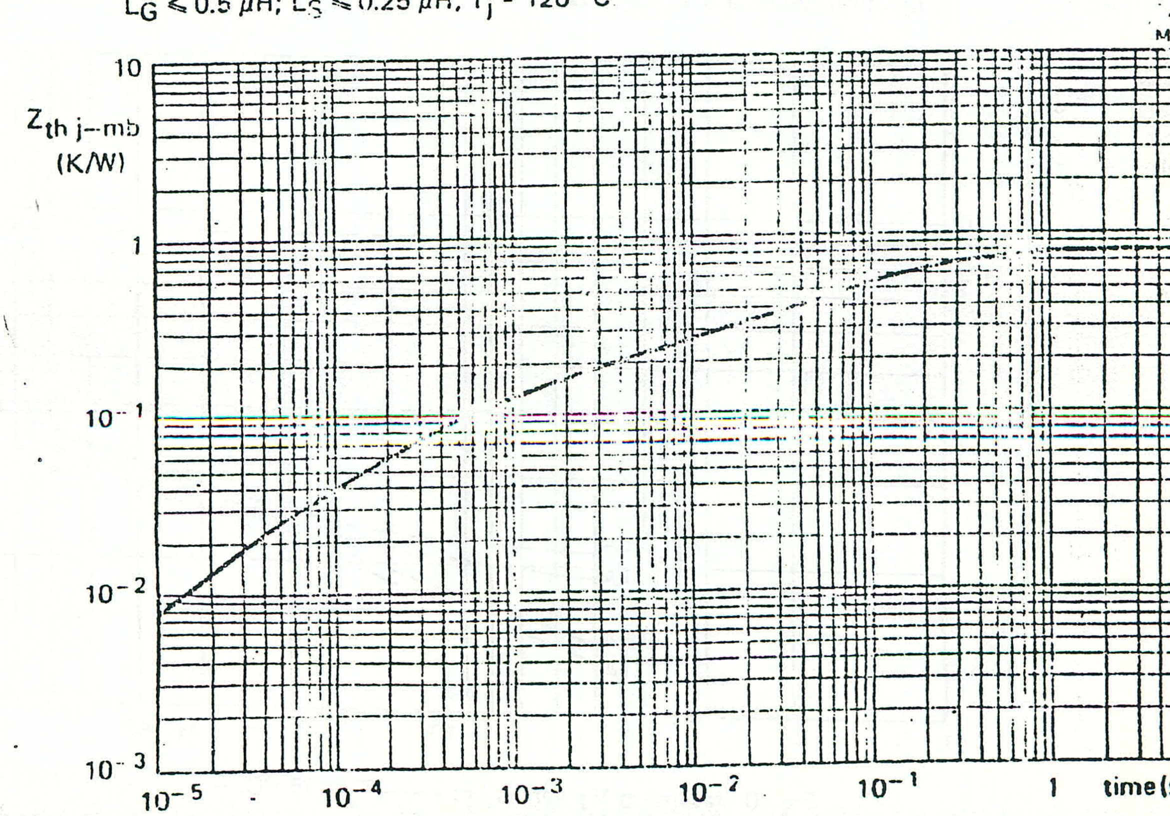


Fig.12 Transient thermal impedance.