CHAPTER 3

CMOS High Speed A/D Converter Architectures

3.1 Introduction

In the previous chapter, basic key functions are examined with special emphasis on the power dissipation associated with its implementation. In this section, several ADC architectures attractive for high speed sampling (> 10MS/s in ~1μm CMOS technology) are discussed in an attempt to illustrate how ADC architectures are evolved from flash to pipeline to reduce its power while increasing the performance. The order of presented ADC architectures is chosen according to author's convenience and may not reflect the actual chronological evolution of ADC architectures.

3.2 Flash Architecture

As shown in Fig. 2, the N bit A/D conversion can be performed in the flash ADC by comparing the applied input signal to the reference voltages generated from a resistor string with ~2^N comparators. The advantage of this architecture is that only one clock cycle is required to perform the A/D conversion. However, the power consumption of this architecture increases exponentially as the resolution increases. For instance, while an 8 bit flash ADC requires 256 comparators, 10 bit requires 1024. In addition, the comparator

offset requirement becomes exponentially more stringent with the resolution; the offset of a 10bit comparator must be less than 1/4 the offset of an 8 bit comparator.

Another big disadvantage is that the input bandwidth is usually much lower than the sampling frequency without a dedicated input S/H circuit. Because the signal source has to drive many comparators implemented in parallel, any mismatch in the signal paths can cause wrong decisions as shown in Fig. 30. This error degrades the overall SNR for

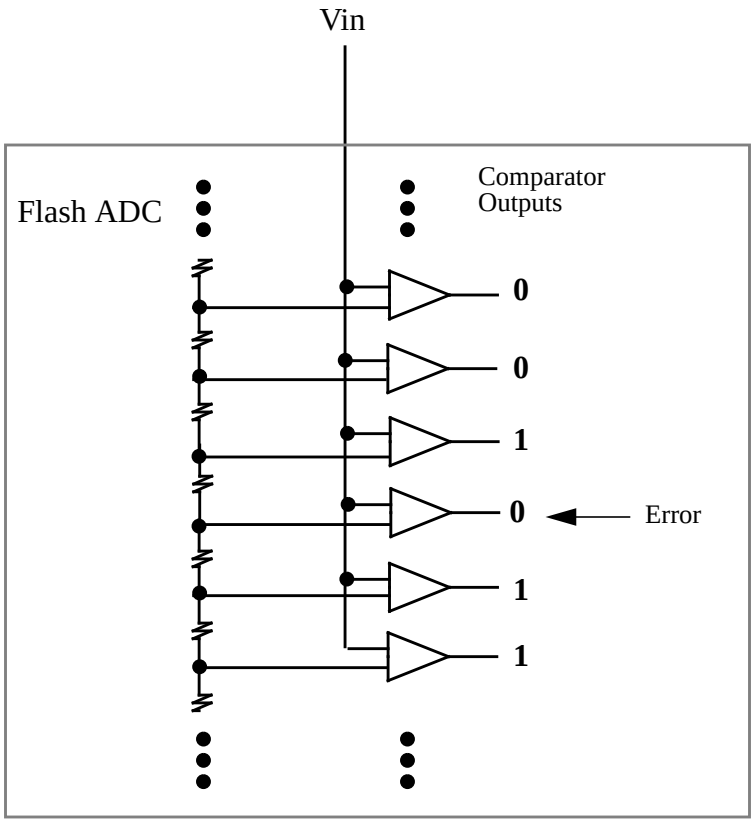

FIGURE 30. A possible error in a flash ADC due to mismatches in signal paths.

the high frequency input signal. At higher resolution, this problem becomes more severe since a large number of comparators laid out over a large area are more subject to process variation and the error budget gets tighter with smaller LSB size.

The most straightforward way to increase the input bandwidth is to use an input S/H circuit as mentioned. Since the stair-case output of the S/H circuit does not change as fast as the continuously varying input signal, the errors made by comparators can be greatly reduced (Fig. 31). The power dissipation of the S/H circuit however will be large in this case, since it has to drive a large input capacitance from many comparators.

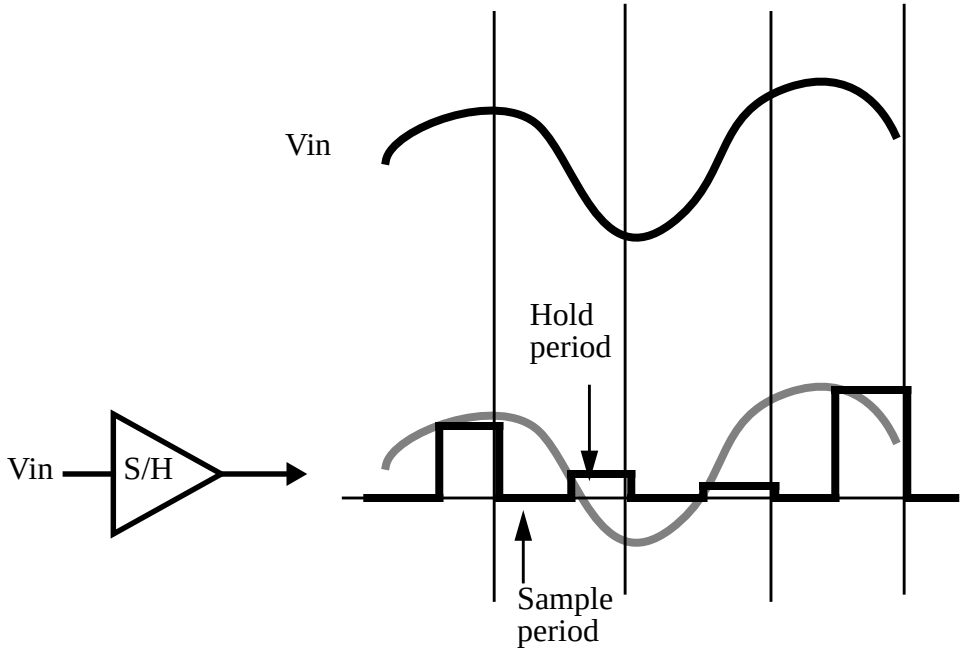

FIGURE 31. A S/H circuit to generate a stair case output.

Therefore, this architecture is only attractive for the low resolution(~6bits or less) applications with high throughput requirement, typically 100MS/sec or higher, as in the disk drive read channel[38][39].

3.3 2 Step Flash Architecture

One way to reduce the number of comparators in the flash ADC is to separate coarse and fine conversions into two time periods. For instance, if the total resolution is 10

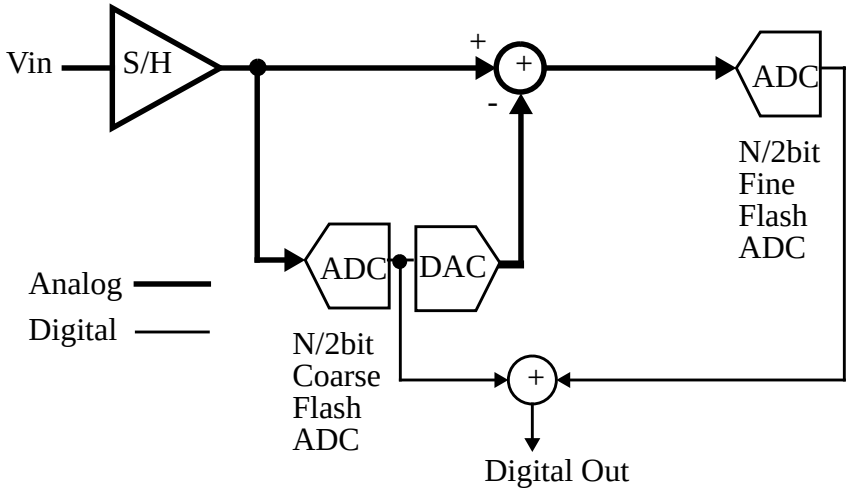

FIGURE 32. A 2 step flash architecture.

bits, the first 5 MSB's can be quantized in the first period and the next 5 MSB's in the next period. Since only 5 bits are quantized in each period, the required number of comparators is about 2^5 in each period, and the total number of comparators is $2x2^5 = 64$ as opposed to 1024 in the straightforward 10bit flash ADC. In this way a substantial amount of comparator power can be saved at the expense of an extra clock cycle.

This architecture is called a "2 step flash[1]", and its conceptual block diagram is shown in Fig. 32. The input signal is first sampled on the sampling capacitor of each comparator in both coarse and fine comparator banks. Then, the coarse conversion is performed by the N/2 bit coarse flash ADC. According to the outcome of the coarse conversion, the quantized signal is subtracted from the input signal, and the residual voltage is again quantized by the N/2bit fine flash ADC. By collecting bits from both

1. Or sometime it is called "subranging".

coarse and fine ADC's, corresponding digital output is generated. During this process, total three clock periods are required per sample for input sampling, coarse conversion, and fine conversion.

One practical implementation is shown in Fig. 33[18][19][21]. Comparators in

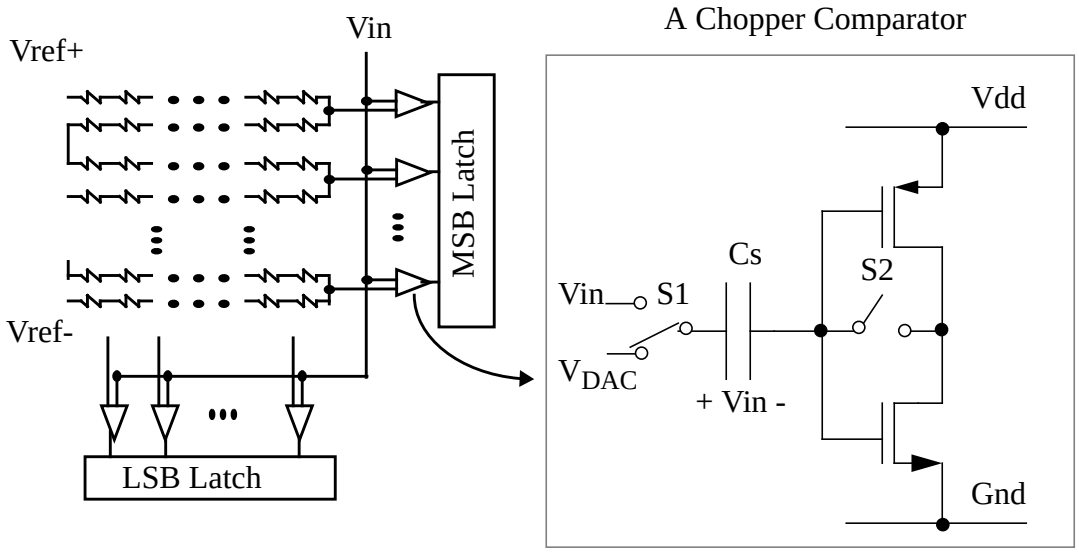

FIGURE 33. A practical implementation of 2 step flash architecture.

flash ADC sections are implemented with CMOS inverters for offset cancellation and compact layout, and reference levels are generated from a resistor string. Instead of using a dedicated S/H circuit as shown in Fig. 32, the S/H function is included within the comparator with the use of its own sampling capacitor, and the input signal is sampled on each and every comparator.

Although the number of comparators are greatly reduced from the flash architecture, path matching is still a major problem, and the input bandwidth is limited to relatively low frequency compared to the conversion rate[18][19][21]. Also, the comparator accuracy must still meet the full resolution requirement, and the offset voltage

of the comparator must be down to 1mV or less for 8-10 bit or higher resolution. As a result, multistage comparators may be required as discussed in the previous section, dissipating large power[18].

One way to relax the comparator accuracy requirement is to use digital error correction[7][8][35]. By making the fine flash ADC section capable of detecting the error due to the comparator offsets in the course ADC section, the coarse comparator requirements can be relaxed. This can be done by including extra comparators at both rails of the fine flash ADC sections as shown in Fig. 34. Therefore, if the comparators in the

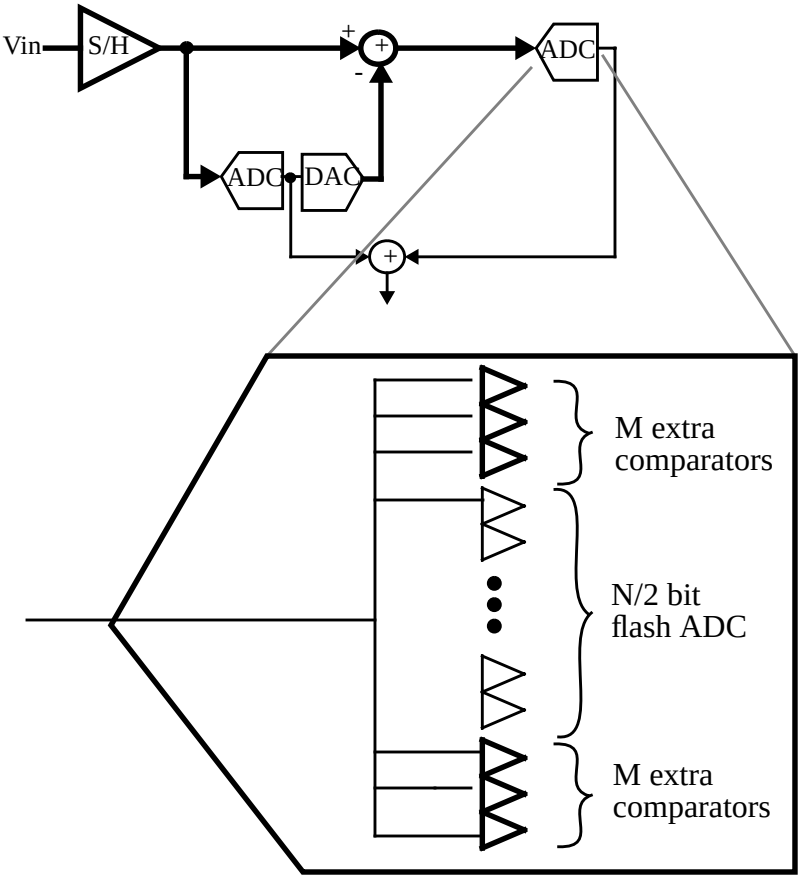

FIGURE 34. Digital error correction with 2M extra comparators in the fine flash ADC section.

coarse flash ADC makes an error and the input to the fine flash ADC goes out of the second stage nominal input range, then the extra comparators at either end detect the overflow level and correct the ADC digital output by digitally adding/subtracting the detected error. The correction range for the comparator offsets in the coarse flash ADC section is ±Mx LSB. So, the use of the digital correction can relax the comparator accuracy requirement of the coarse flash ADC section. However, the accuracy of the fine flash ADC section is still required to the full ADC resolution to make an error detection.

Fine comparators accuracy requirements can be relaxed by including an interstage gain amplifier to amplify the signal for the fine comparator bank as shown in Fig. 35

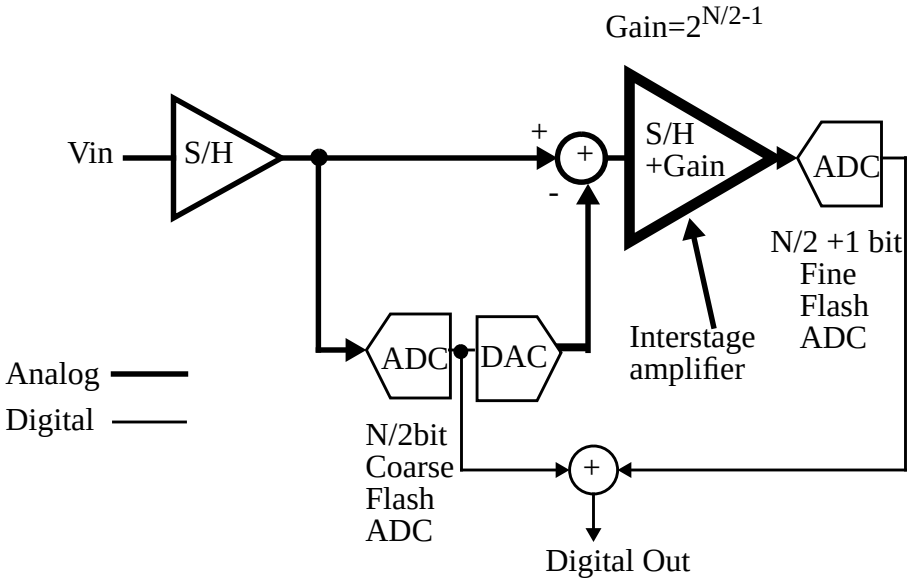

FIGURE 35. A 2 step flash ADC with an interstage amplifier.

[22][23]. By amplifying the signal, the accuracy requirements for fine conversion comparators are relaxed by the gain of the interstage amplifier, $2^{N/2-1}$. Here, the gain of $2^{N/2-1}$ is deliberately used instead of $2^{N/2}$ in order to prevent the over-range problem mentioned earlier, and the resolution of the fine flash ADC is increased by 1. Then, instead of using N/2 bit ADC with N bit offset requirements, an N/2 bit coarse flash ADC with N/

2 bit offset requirements (N/2+1 bit offset requirements for N/2+1 bit fine flash section) can be used[22].

Another advantage of this configuration is that the conversion steps can be pipelined due to the S/H interstage amplifier; while the first stage flash ADC works on the most recent sample, the second stage flash can concurrently work on the previous sample. As opposed to three clock periods in the previous scheme, only two clock periods are required for sampling and quantization, and in turn the throughput can be increased.

However, an op amp must be used for the S/H/Gain block and its power can be significant if fast output settling is required. While the input S/H function can be included in the comparator with the use of a sampling capacitor, the interstage amplifier must be implemented with a SC circuit which usually requires an op amp. Since it has to drive $2^{N/2+1}$ comparators in the fine flash ADC section, the op amp will dissipate large power if N is large.

3.4 Pipeline Architecture

In the 2step flash architecture with an interstage amplifier presented in the previous section, the accuracy requirements of the comparators are relaxed at the expense of the op amp power in the SC circuit. One interesting question to ask here is what happens if more interstage amplifiers are included to further relax the comparator requirements. This is the basic idea behind the pipeline architecture in relation to the power dissipation.

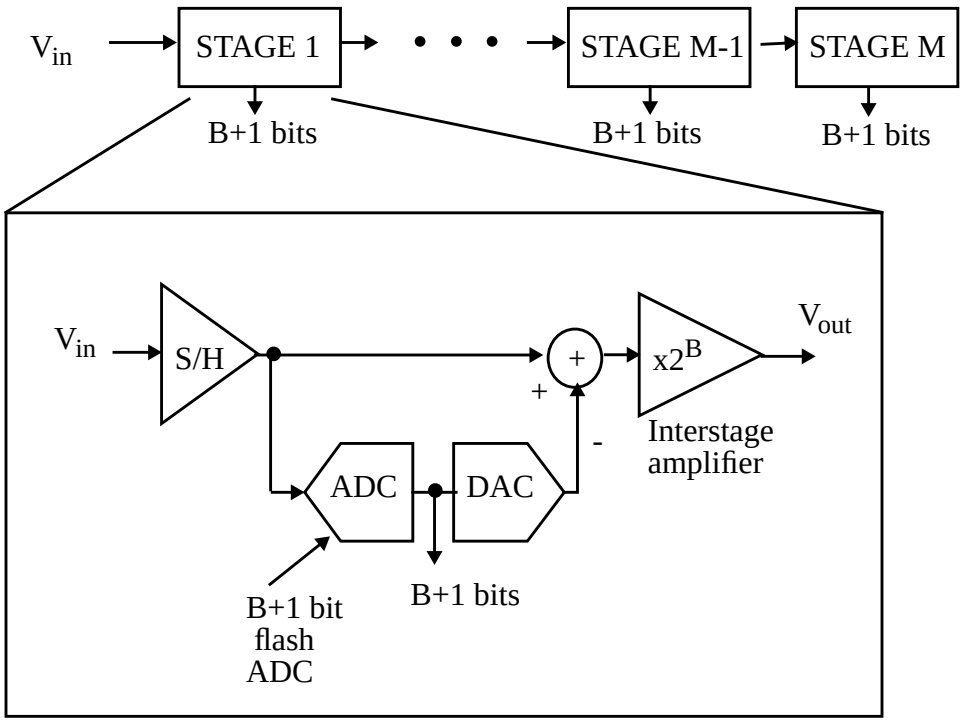

FIGURE 36. A typical pipeline architecture.

In Fig. 36, a basic schematic for a pipeline architecture is shown. Each stage samples the signal from the previous stage and it quantize to B+1 bits by the flash ADC section. Then, the quantized signal is subtracted and the residue is amplified through the interstage amplifier to be sampled by the subsequent stage. The same procedure is repeated in each stage down the pipeline to perform A/D conversion. The number of comparators required in this case is the number of stages times the number of comparators in each stage. From Fig. 36, it is roughly $(Mx2^{B+1})$[1]. The required number of stage is approximately the ADC resolution divided by effective per-stage resolution. Effective per-stage resolution here is denoted with B, and one extra bit is used for digital correction.

1. Number of comparators per stage can be even further reduced in actual implementation. Only general discussion is presented here from power dissipation perspective. For more detailed discussion on the pipeline architecture, see Chapter 5.

As discussed earlier, the flash ADC section in each stage has to meet only B+1 bit requirement due to the interstage gain and digital correction. Therefore, the lower B is, the more the comparator requirement gets relaxed.

Another observation is that both interstage amplifier and DAC requirements get relaxed down the pipeline. For instance, if the ADC resolution is 10bit and B=1, then while the first stage has to meet 10bit requirement, the requirement on the second stage is relaxed by 1bit. This implies potential power saving since the S/H circuits in later stages can be scaled down with smaller sampling capacitors due to relaxed accuracy requirements. The number of comparators are further reduced from 2step flash architecture at the expense of increased latency and required S/H circuits. Also, the circuit complexity grows approximately linear compared to exponential growth in flash and 2step flash architectures.

3.5 Power Comparison

Up to now, only general descriptions of three high speed ADC architectures in CMOS are reviewed in terms of the power dissipation. Detailed comparison of the power dissipation between different architectures is not easy because it involves a number of variables including resolution/sampling rate, the choice of technology, variations within the same architecture, etc. and many corresponding assumptions are needed in order to proceed with the analysis. Also, since there are many variations possible within each architecture itself, the result of the analysis based on the basic architecture may not apply to practical situations.

One way to look at the power consumption of different architectures is therefore to look at the *power factor*, meaning *what fraction of the circuits in the whole system has to meet what resolution requirement*. This is *based on the assumption that the accuracy*

requirement and the power consumption of a component are approximately proportional to each other, as discussed in previous sections.

For flash architecture, for example, the power factor of the architecture is 100%, since each and every comparator and DAC have to meet the full resolution requirement.

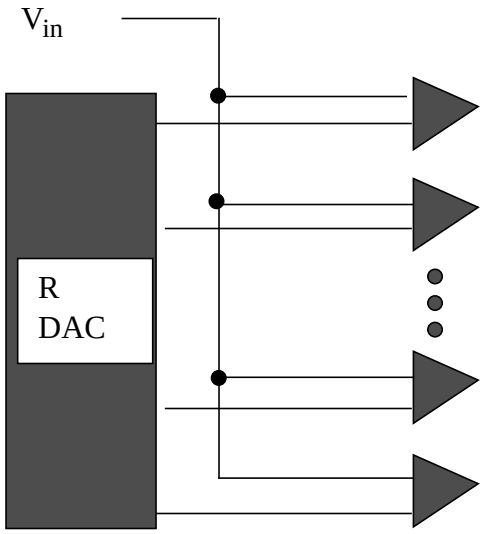

FIGURE 37. Flash architecture's power factor: the shaded region indicates full resolution requirements.

For a 2step flash architecture, the power factor of the architecture can be made less

than 100% as illustrated in Fig. 38. While both DAC and fine ADC section require full

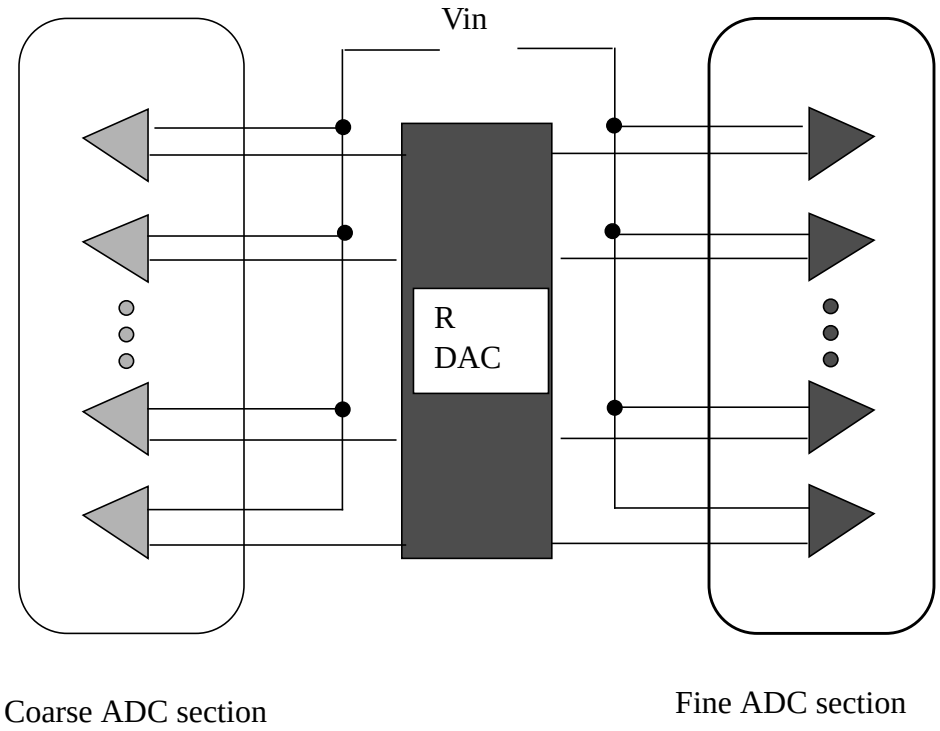

FIGURE 38. Illustration of the power efficiency of a 2 step flash architecture. Darker shaded region indicates more stringent accuracy requirement.

resolution requirement, the coarse ADC section requirement can be relaxed with the digital error correction. The level of error tolerance on the coarse ADC section depends on how much digital error correction range the fine ADC section can provide as explained in section 3.3, and the correction range varies from +/-3 LSB's in [24] to a much larger value in [22],[23] with a S/H interstage amplifier.

On the other hand, in pipeline architecture, the stage resolution decreases in later

stages as discussed earlier as illustrated in Fig. 39. While the flash section has a fixed

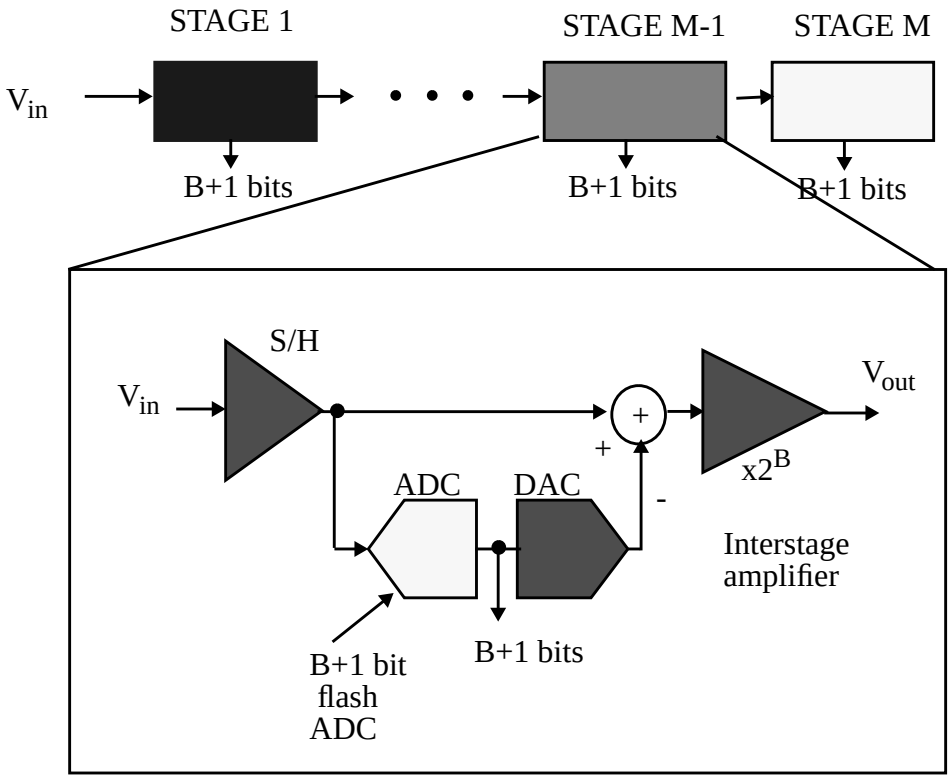

FIGURE 39. Illustration of the power factor of a pipeline architecture. Darker shaded region indicates more stringent accuracy requirement.

resolution requirement of B+1 bit, requirements on the interstage amplifiers and DAC section are relaxed in later stages. Among these three architectures, the power factor is therefore lowest. However, again, this power factor comparison presents a highly qualitative description of how each architecture is utilizing each key building block, not an absolute comparison.

3.6 Other ADC Architectures

Other widely used ADC architectures in CMOS technology are algorithmic, successive approximation, and Σ-Δ converters. All of these architectures are used for relatively low speed operation requiring many clock cycles to perform the A/D conversion, but their advantages are small area for the algorithmic converter and high dynamic range for successive approximation converter and Σ-Δ oversampled converter.

An algorithmic converter can be thought of as a pipeline A/D converter implemented in a recirculating manner as shown in Fig. 40. Input signal is first sampled at

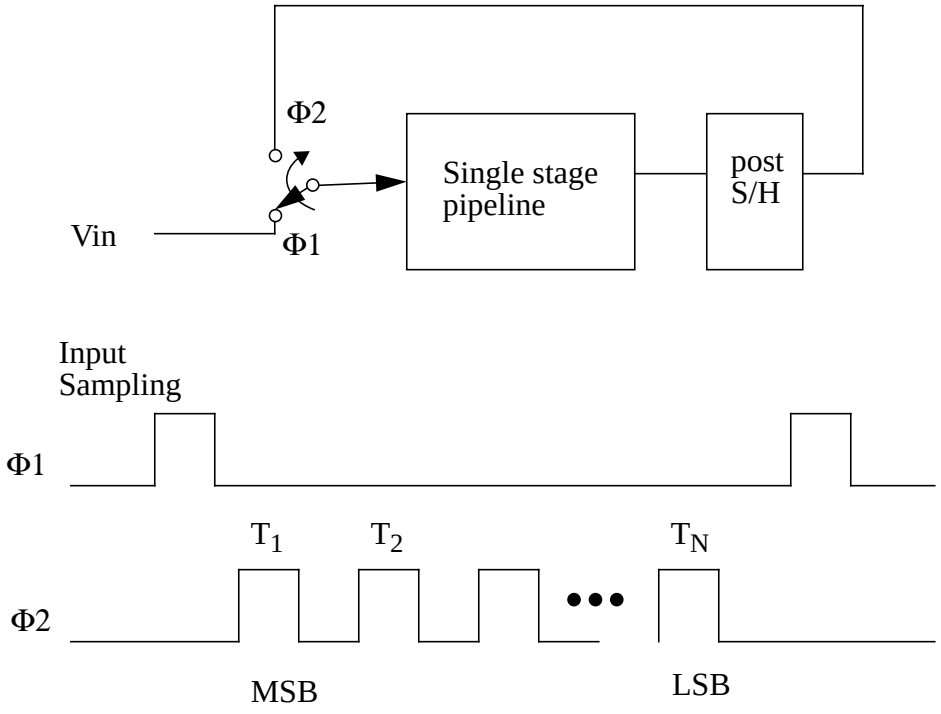

FIGURE 40. An algorithmic A/D converter.

the beginning of a clock cycle. Then, the A/D conversion is performed on the MSB. In the next clock period, the post S/H circuit samples/feeds back the residue from the output of the single pipeline stage back to its input. The pipeline stage then resolves the next

significant bit and the same procedure repeats till the last bit.

Power factor of this architecture, according to the definition presented in section 3.5, is close to 100%. Since the same SC circuit in the single pipeline stage is used repeatedly during all conversion periods from T_1 to T_N, it has to satisfy the most stringent accuracy requirements for the initial MSB conversion. However, since this architecture does not require many stages, it is good for the applications where small area is required with relatively low sampling rates of ~1MS/s. Although N N-bit parallel algorithmic converter stages can achieve the same throughput as a single N-bit pipeline A/D converter, the larger power consumption than a single N bit pipeline ADC running N times faster is expected due to its near 100% power factor even without considering power from the post S/H circuit and path matching. Examples can be found in [27][35].

A successive approximation converter shown in Fig. 41 usually dissipates a very

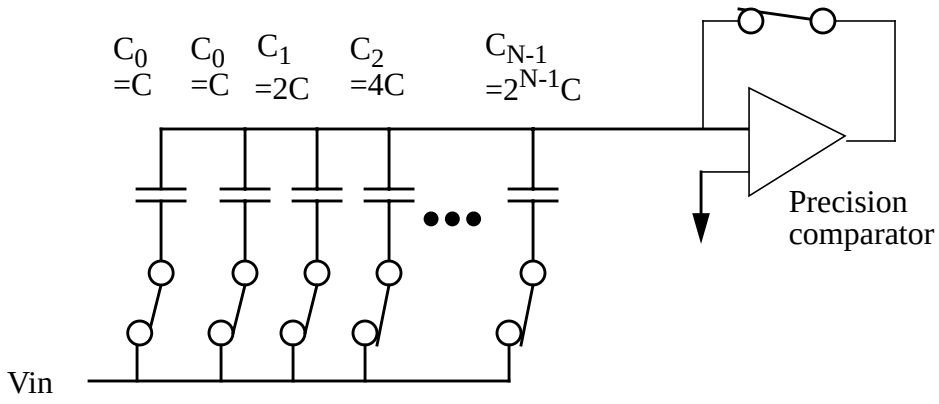

FIGURE 41. A successive approximation A/D converter core circuit.

low DC power mostly from the bias current of a single precision comparator; the rest of the power dissipation is purely dynamic from capacitive switching excluding the DAC power. The S/H function can be incorporated with the binary capacitor array requiring no

SC type of op amp based S/H circuit with DC power. Power factor of this converter is still close to 100%; the comparator offset and sensitivity has to be of full accuracy since the same comparator is used repeatedly, and the C-DAC during each clock period has to settle to a full accuracy.

The dynamic power in the C-DAC can be reduced by reducing the total capacitance by using T-network as shown in Fig. 42. By using a proper value of Catt,

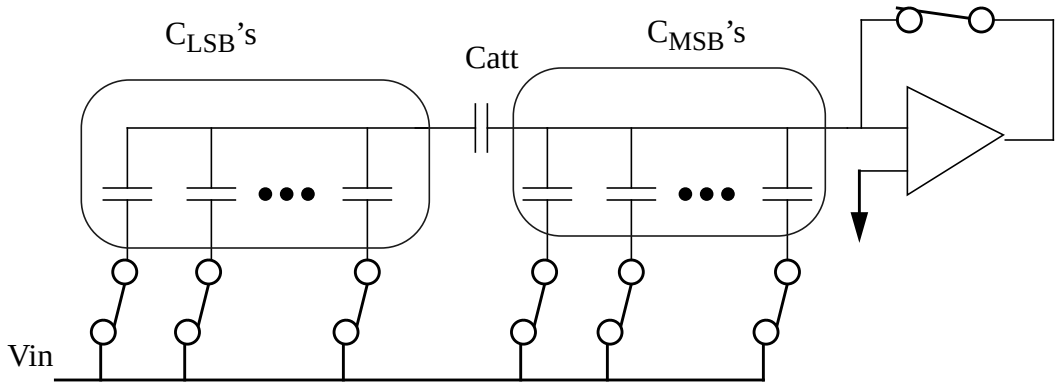

FIGURE 42. A T-network for C-DAC in a successive approximation ADC.

C_{LSB}'s on the left side of Catt can be effectively attenuated by the series capacitance divider effect. If kT/C noise is not a concern, this technique allows to use smaller capacitors for C-DAC. However, reliably controlling Catt and other parasitic capacitance in as-fabricated state is almost impossible and careful calibration/trim is required[36]. According to the definition, the power factor of a T-network successive approximation ADC does not change.

A first order Σ-Δ oversampled A/D converter architecture is shown in Fig. 43. In

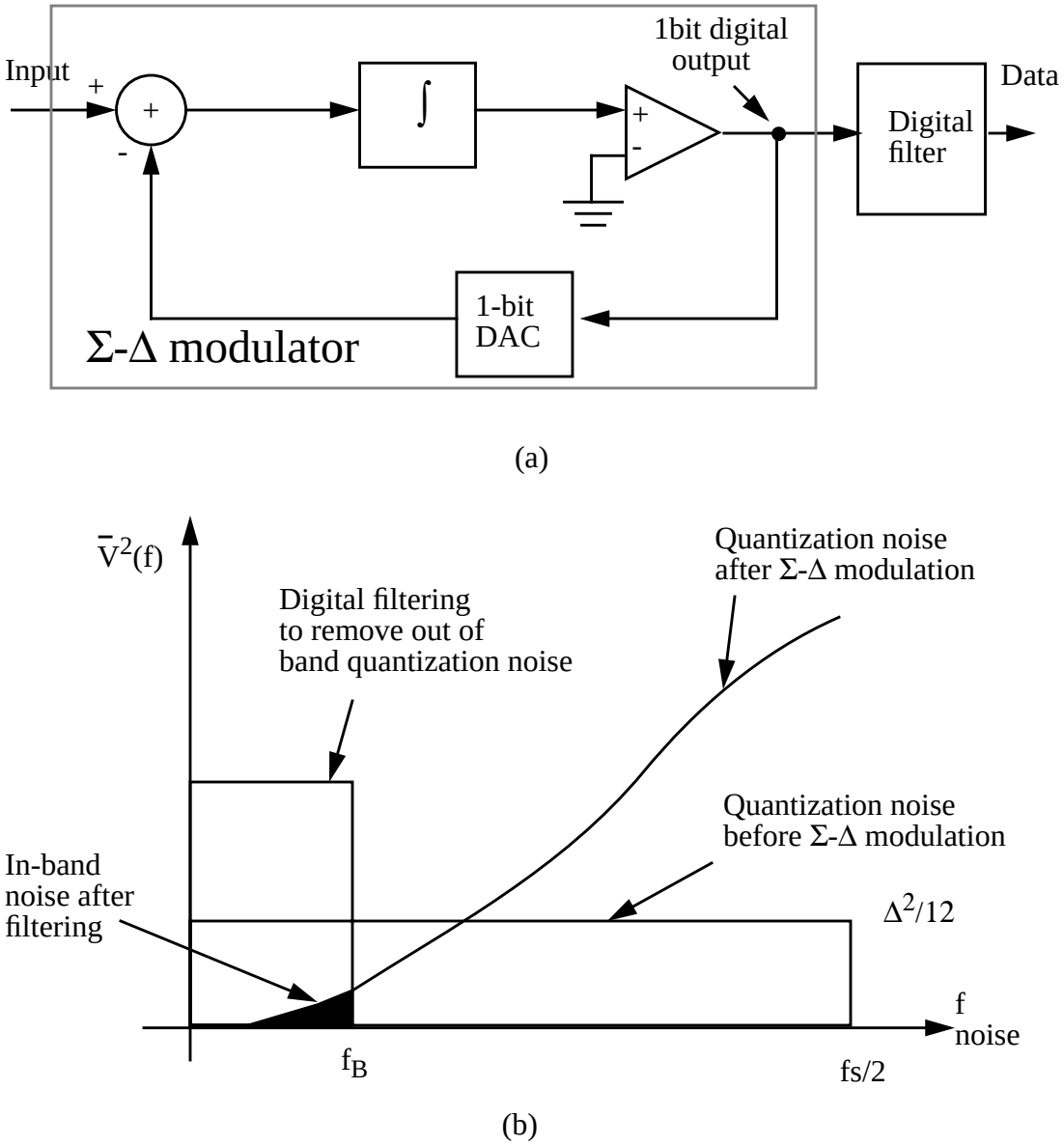

FIGURE 43. (a) Block diagram of a first-order Σ–Δ modulator (b) Modulator output spectrum.

this architecture, the frequency response of the quantization noise is reshaped in order to transfer most of its energy to higher frequencies by proper oversampling and negative feedback. Then, the noise is filtered out by the digital low pass filter leaving only a small portion of the quantization noise. The ratio of the sampling rate(fs) to the signal bandwidth

(f_B) is called the oversampling ratio, and the SNR improvement with the increase in its oversampling ratio is 9dB per octave for quantization noise and 3dB per octave for thermal noise due to straightforward averaging.

The integrator in the first order Σ-Δ modulator can be implemented in a SC circuit configuration as shown in Fig. 44. Power dissipation of this SC circuit depends on the

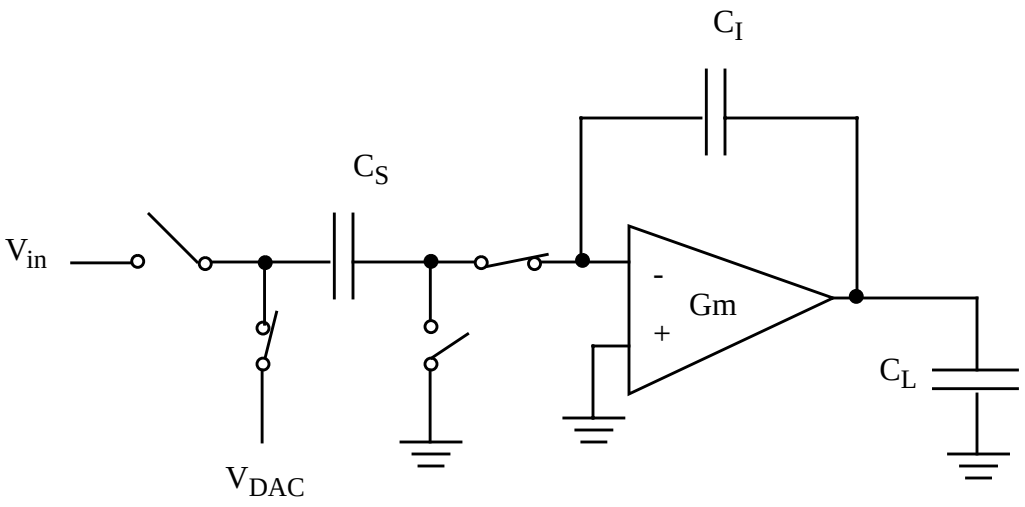

FIGURE 44. A simplified schematic for the SC implementation of the first order Σ-Δ modulator.

oversampling ratio and the size of the capacitor. If the oversampling ratio is M, the output of this integrator has to settle with a bandwidth, $(Gm \cdot f)/C_L$, where Gm is the overall transconductance of the op amp and C_L is the total output load capacitance. Since the kT/C noise on the sampling capacitor gets reduced by factor of M due to oversampling, the capacitors can be reduced by the same ratio if the same amount of kT/C noise for a Nyquist converter is to be allowed. However, since the SC circuit now has to operate M times faster, the same Gm is required as before, and as a result there's no net power saving compared to the front end S/H of the Nyquist converter if power from op amp bias current

is assumed to be approximately proportional to Gm.

Higher order loops can be used to reduce the oversampling ratio while achieving the same dynamic range. However, in addition to the increased number of modulator stages, more complex digital filter section is also required with possibly more power dissipation. Power factor is difficult to define here since the digital power dissipation must be included. However, it can be noted that the power dissipation in the Σ-Δ modulator is comparable but not much less than that of the S/H of the Nyquist converter, based on the argument given above.

In terms of practical considerations, tolerance on various component matching and relaxed requirement on the anti-aliasing filter make the Σ-Δ architecture more attractive for high resolution (above 12 bits) A/D converters than other architectures.