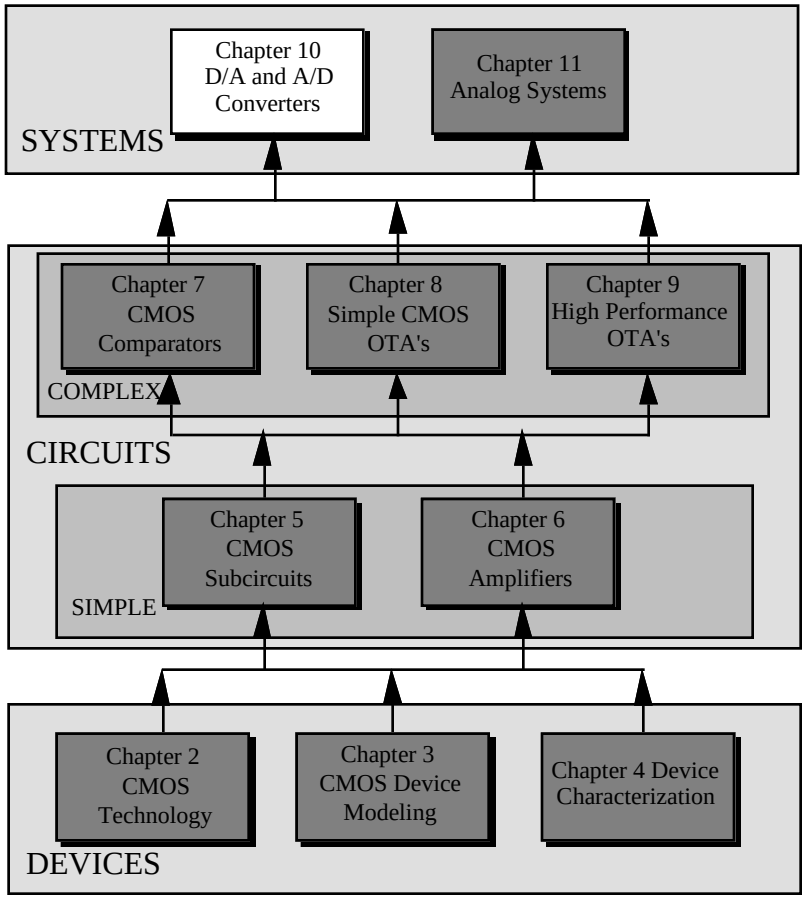
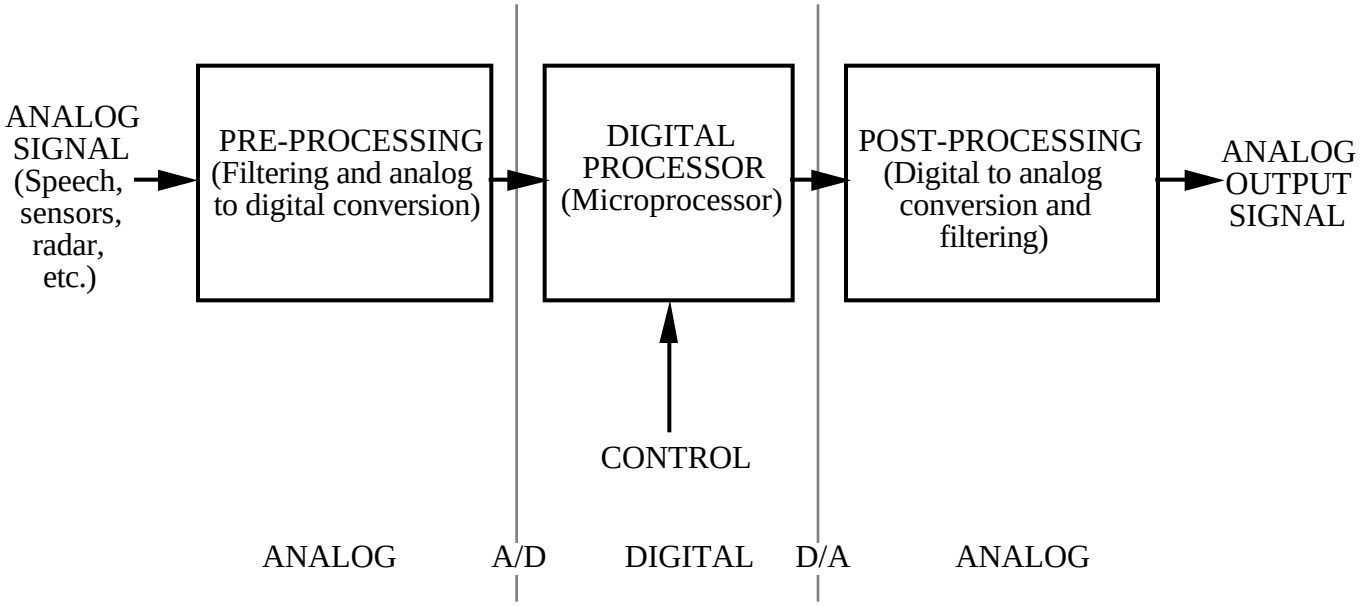
X. CMOS DATA CONVERTERS

Contents

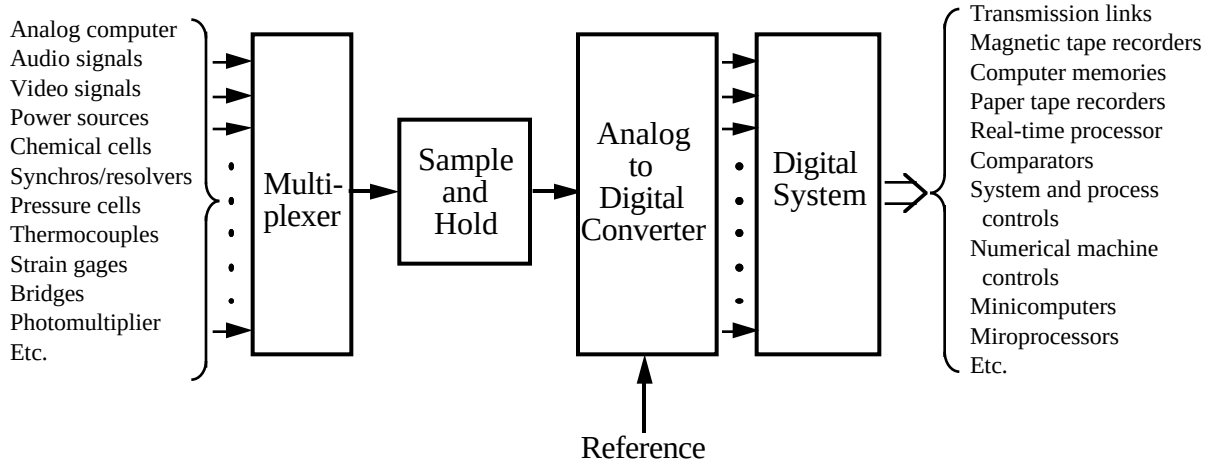
Organization

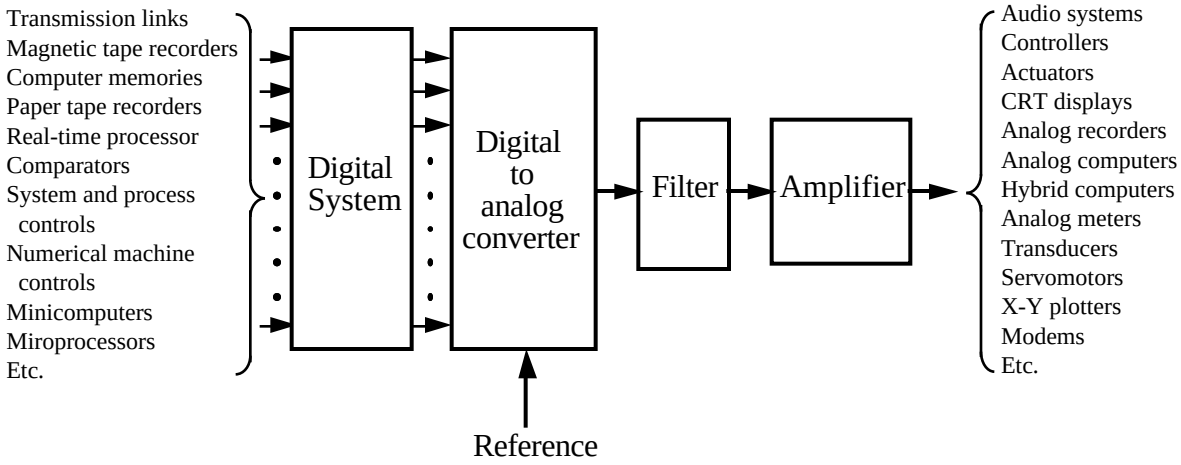


Importance of Data Converters in Signal Processing



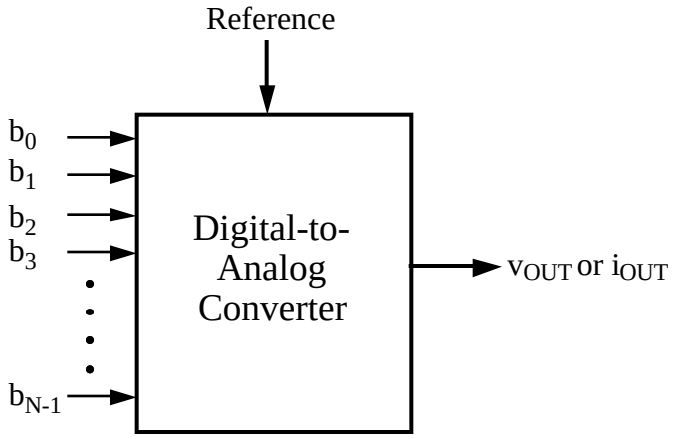
A/D and D/A Converters in Data Systems





X.1 - CHARACTERIZATION AND DEFINITION OF CONVERTERS

General Concept of Digital-to-Analog (D/A) Converters



$$v_{OUT} = KV_{ref}D \quad \text{or} \quad i_{OUT} = KI_{ref}D$$

where

K = gain constant (independent of digital input)

$$D = \frac{b_0}{2^N} + \frac{b_1}{2^{N-1}} + \frac{b_2}{2^{N-2}} + \cdots + \frac{b_{N-1}}{2^1} = \text{scaling factor}$$

V_{ref} (I_{ref}) = voltage (current) reference

b_{N-1} = most significant bit (MSB)

b_0 = least significant bit (LSB)

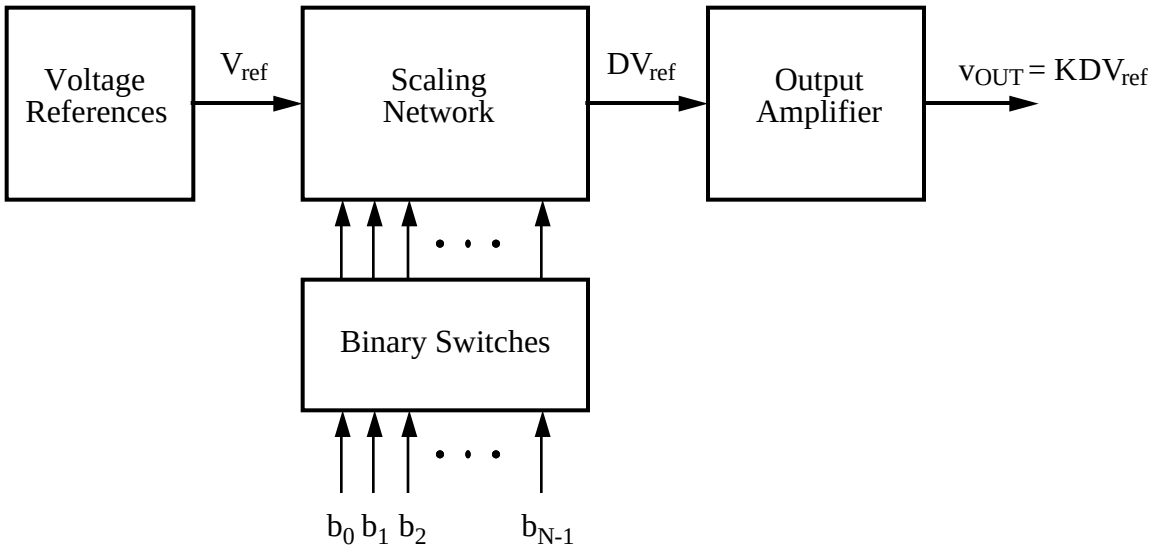
For example,

$$v_{OUT} = KV_{ref}\left(\frac{b_0}{2^N} + \frac{b_1}{2^{N-1}} + \frac{b_2}{2^{N-2}} + \cdots + \frac{b_{N-1}}{2^1}\right)$$

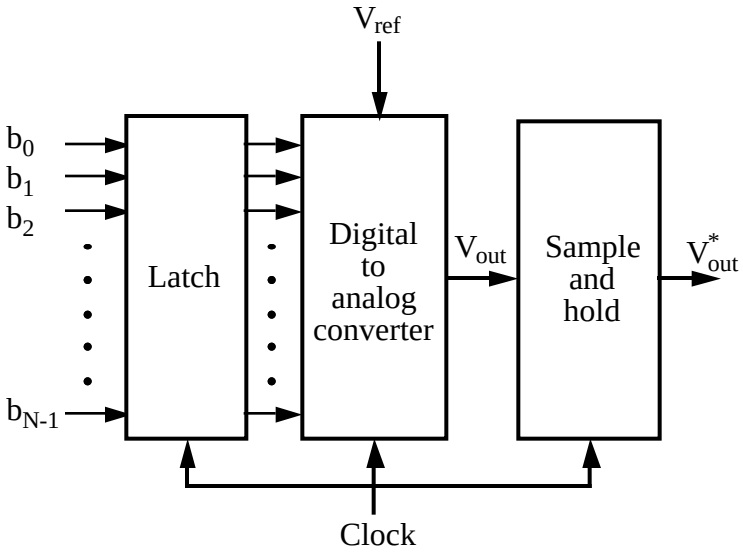
$$= KV_{ref}\frac{1}{2^N}\sum_{j=0}^{N-1} b_j 2^j$$

Basic Architecture of a D/A Converter

Continuous Time D/A Converter-

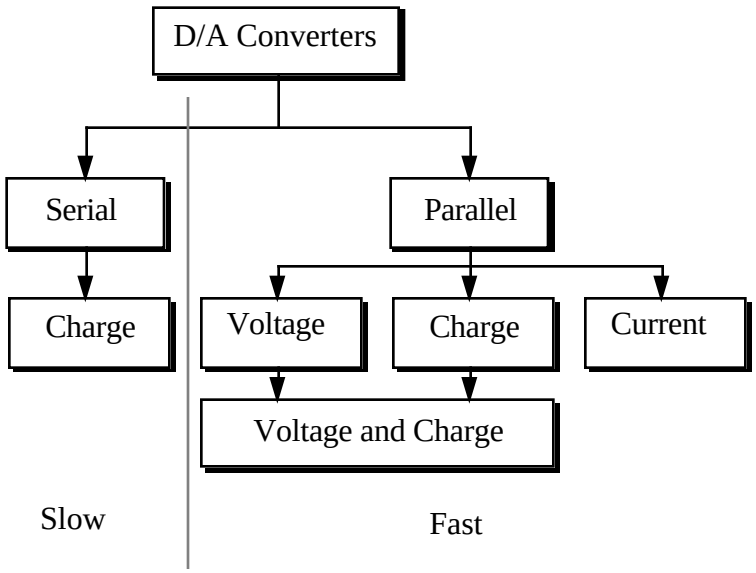


Clocked D/A Converter-



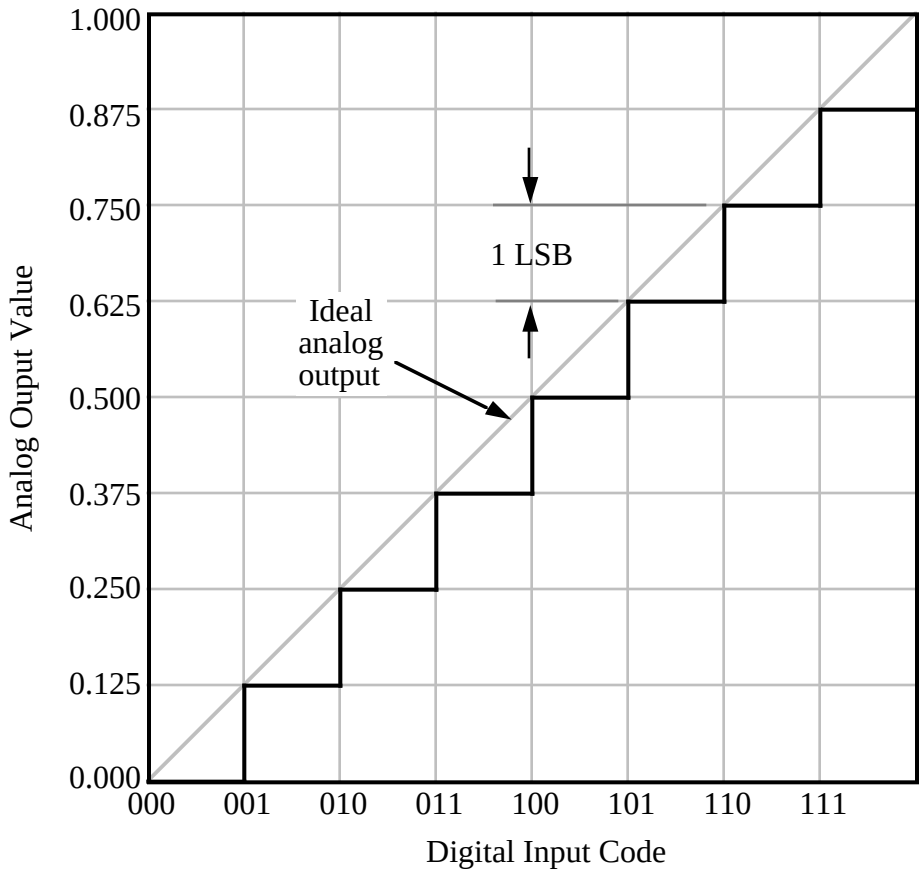
Classification of D/A Converters

Done by how the converter is scaled-



Static Characterization of D/A Converters

Ideal input-output D/A converter Static Characteristic -

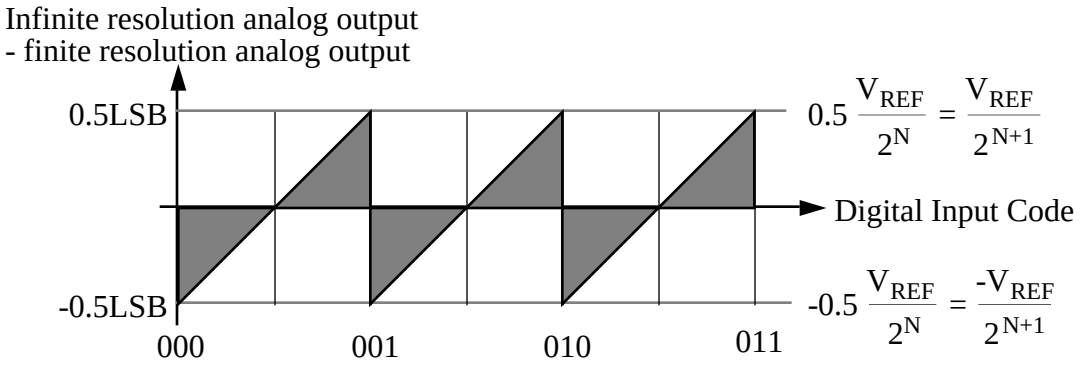


An ideal LSB change causes an analog change of $\frac{V_{ref}}{2^N}$

Definitions

Resolution is the smallest analog change resulting from a 1 LSB digital change (quantified in terms of N bits).

Quantization Noise is the inherent uncertainty in digitizing an anlog value with a finite resolution converter.



Dynamic range (DR) is the ratio of FS to the smallest resolvable difference.

$$DR = \frac{FS}{\text{LSB change}} = \frac{V_{REF}\,\frac{2^N - 1}{2^N}}{V_{REF}\,\frac{1}{2^N}} = 2^N - 1$$

$$DR(dB) = 20\log_{10}(2^N - 1) \cong 6N \text{ dB}$$

Signal to noise ratio (SNR) for a sawtooth waveform
Approximating $FS = LSB(2^N - 1) \cong LSB(2^N)$,

$$SNR = \frac{\text{Full scale RMS value}}{\text{RMS value of quantization noise}} = \frac{\frac{2^N}{2\sqrt{2}}}{\frac{1}{\sqrt{12}}} = \frac{\sqrt{12}}{2\sqrt{2}}\,2^N$$

$$SNR\,(dB) = 20\log_{10}\left[\left(\frac{\sqrt{6}}{2}\right)2^N\right] = 20\log_{10}\left(\frac{\sqrt{6}}{2}\right) + 20\log_{10}(2^N)$$

$$= 20\log_{10}(1.225) + 6.02N = 1.76 \text{ dB} + 6.02N \text{ dB}$$

Definitions - Continued

Full scale (FS) is the the maximum DAC analog output value. It is one LSB less than V_{REF} .

$$FS = V_{REF}\frac{2^N - 1}{2^N}$$

A *monotonic* D/A (A/D) converter is one in which an increasing digital input code (analog input) produces a continuously increasing analog output value (digital output code).

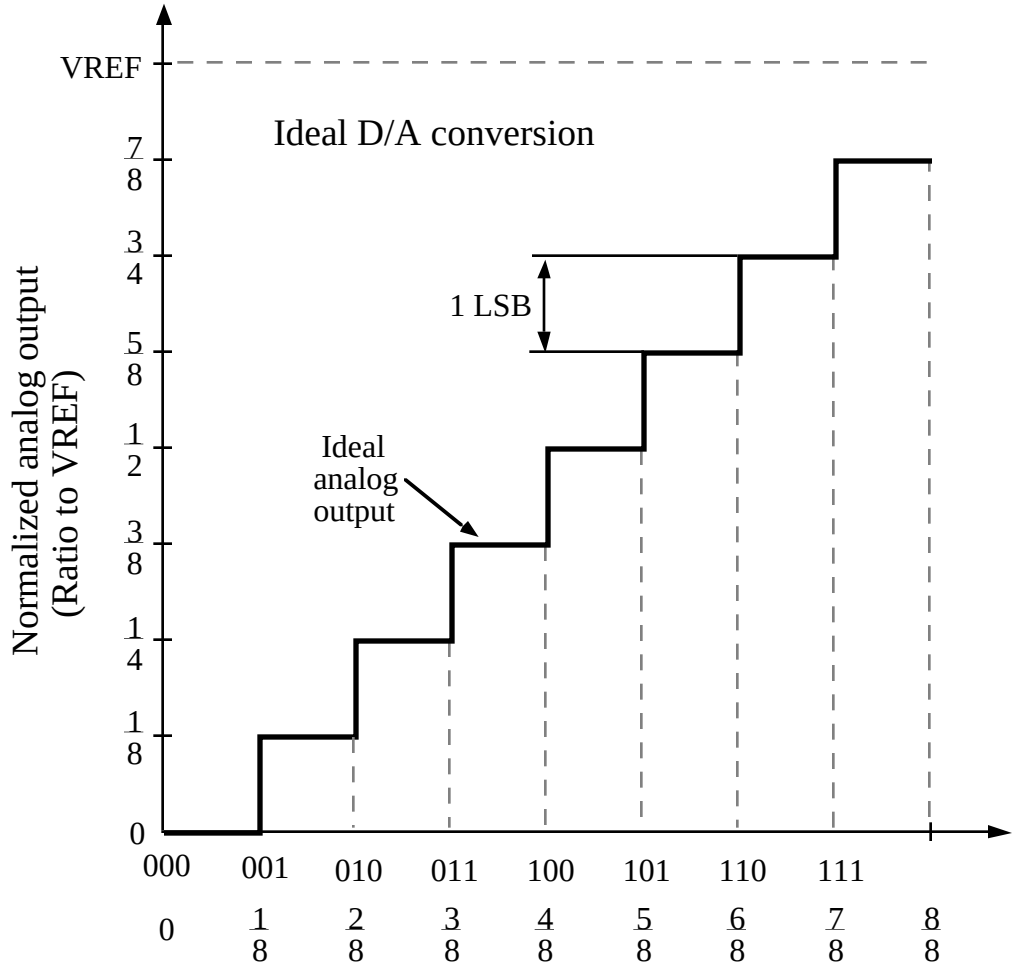
Offset error is a constant shift of the actual finite resolution characteristic from the ideal infinite resolution characteristic.

Gain error is a deviation between the actual finite resolution characteristic and the ideal infinite resolution characteristic which changes with the input.

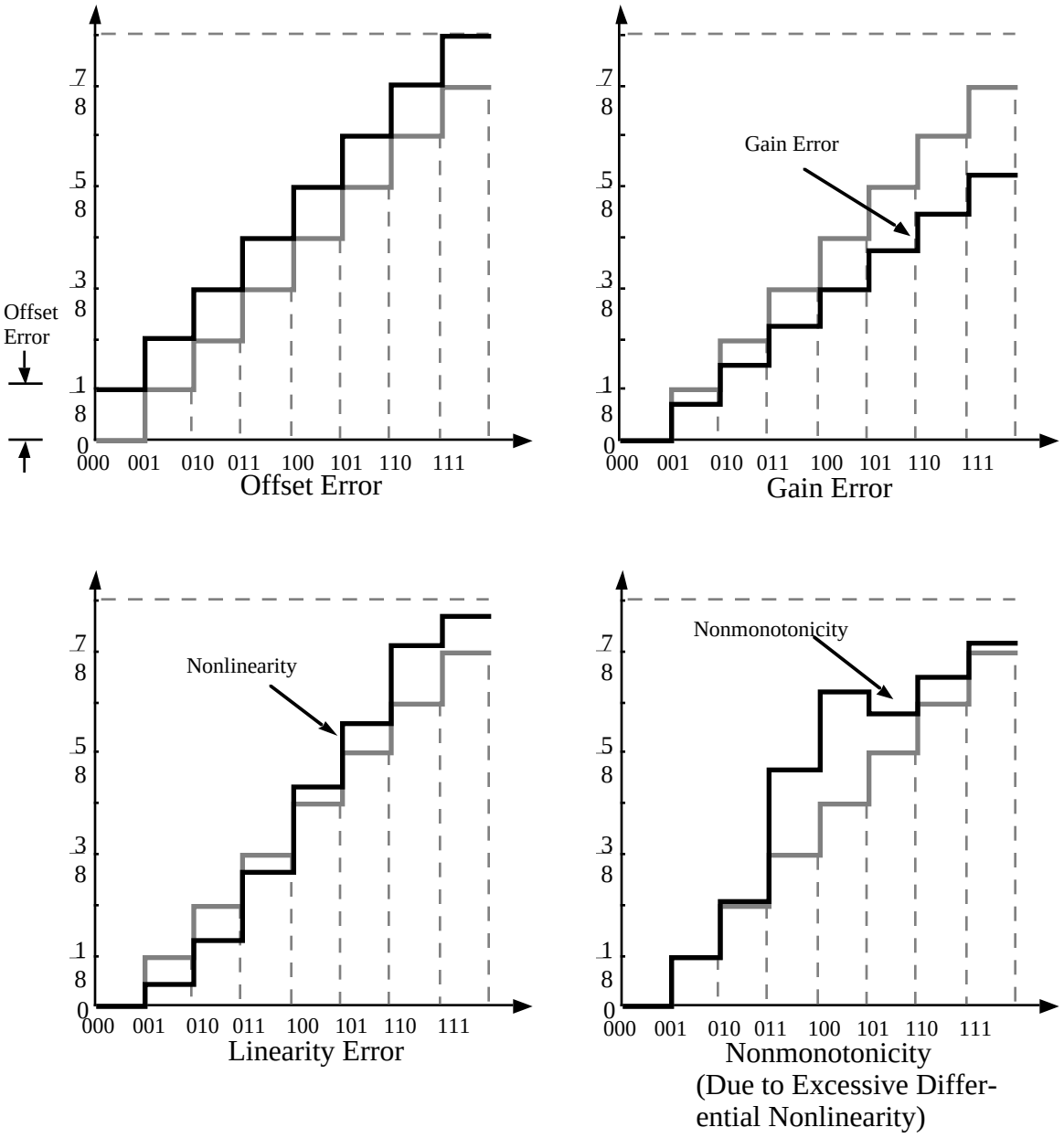
Integral nonlinearity (INL) is the maximum difference between the actual finite resolution characteristic and the infinite resolution characteristic.

Differential nonlinearity (DNL) is the maximum deviation of any analog output changes caused by an input LSB change from its ideal change of $\frac{FS}{2^N}$.

3-BIT D/A CONVERTER ILLUSTRATION



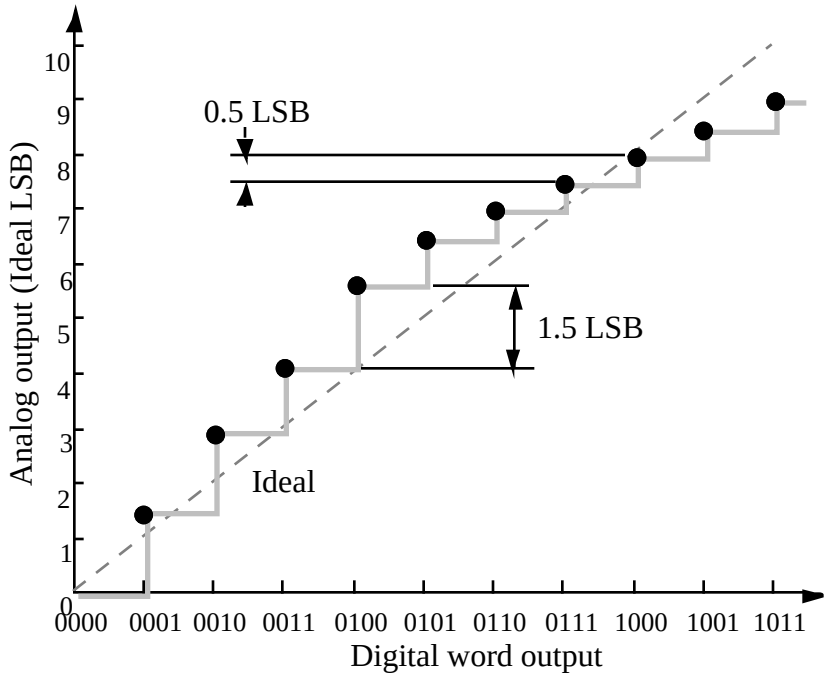
Ideal relationship



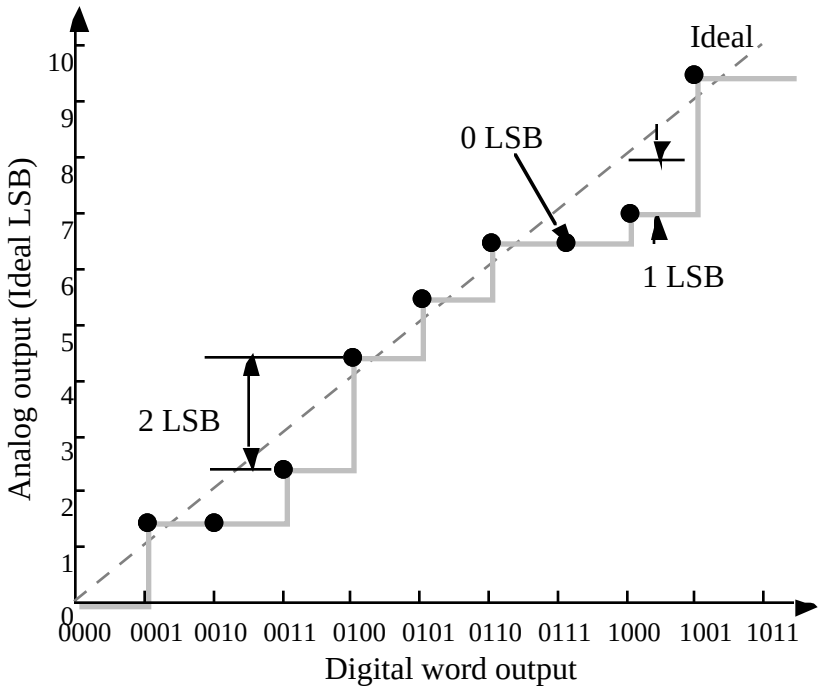
Typical sources of errors

Integral and Differential Linearity for a D/A Converter

D/A Converter with ±1.5 LSB integral nonlinearity and ±0.5 LSB differential nonlinearity



D/A converter with ±1 LSB integral nonlinearity and ±1 LSB differential nonlinearity



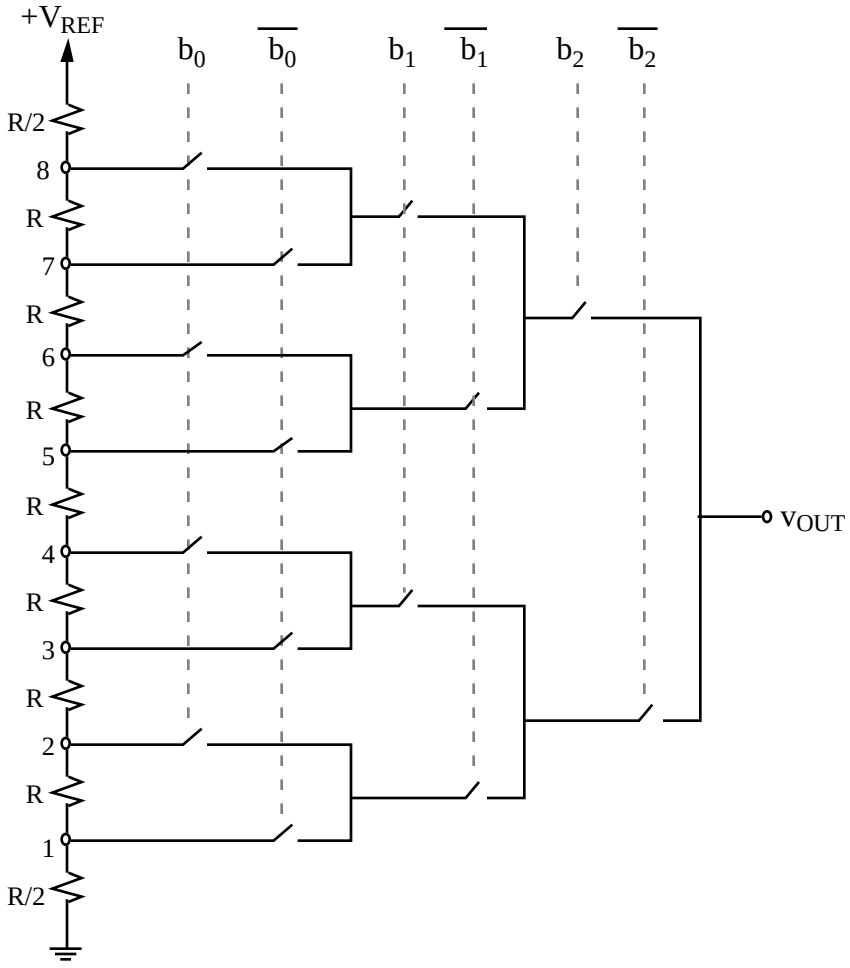
X.2 VOLTAGE SCALING CONVERTERS

3-BIT VOLTAGE SCALING D/A CONVERTER

Assume that $b_0 = 1$, $b_1 = 0$, and $b_2 = 1$

MSB: b_2

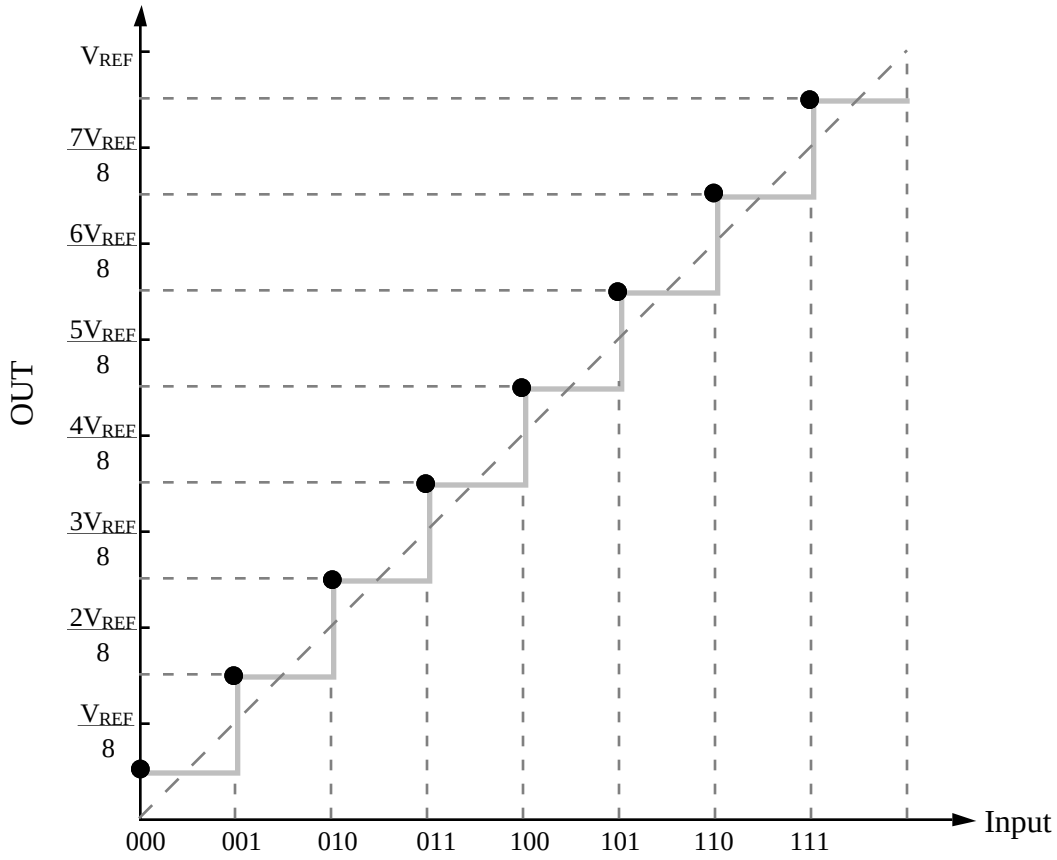
LSB: b_0



$$v_{OUT} = \frac{V_{REF}}{8}(D+0.5) = \frac{V_{REF}}{16}(2D+1) = 0.6875V_{REF} = \frac{11}{16}V_{REF}$$

3-BIT VOLTAGE SCALING D/A CONVERTER - CONT'D

Input-Output Characteristics:



Advantages:

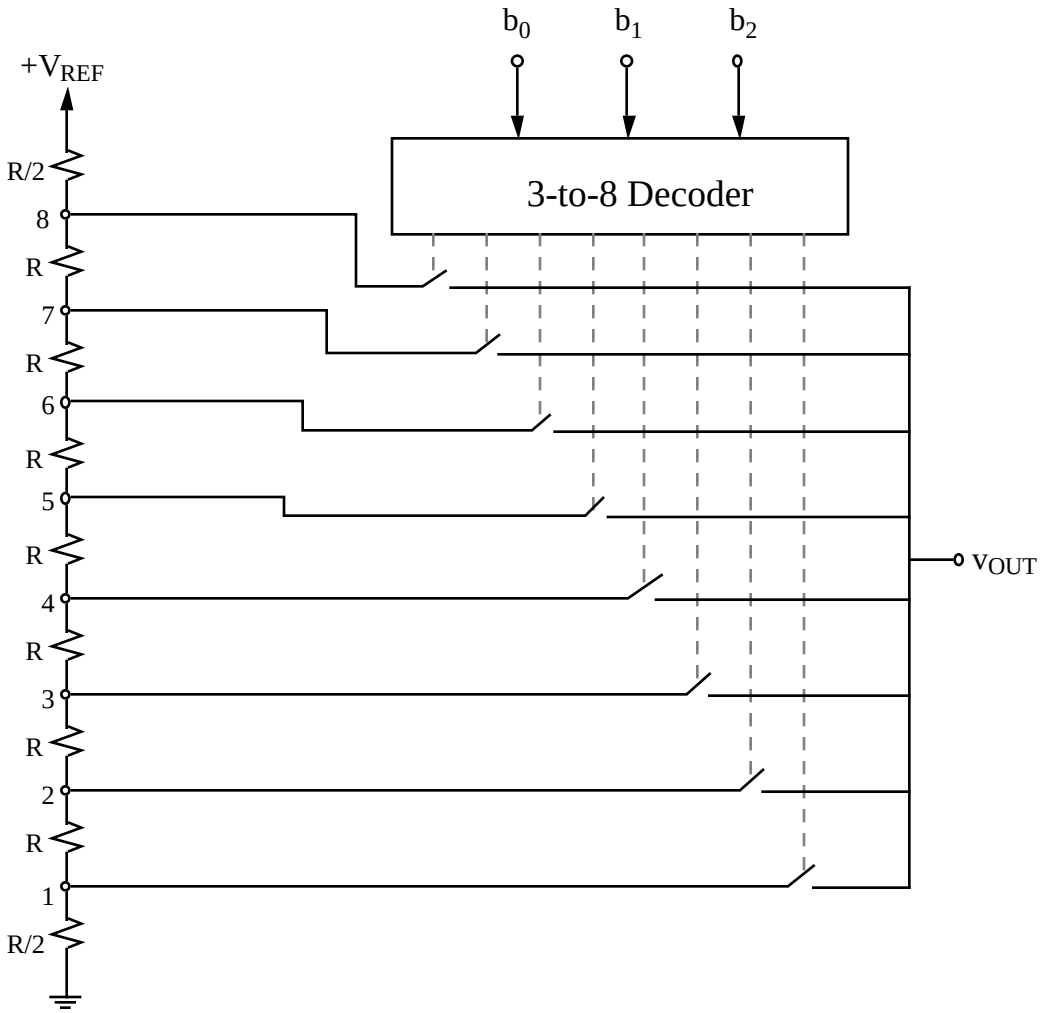
- Inherent monotonicity
- Compatible with CMOS technology
- Small area if n < 8 bits

Disadvantages:

- Large area if n > 8 bits
- Requires a high input impedance buffer at output
- Integral linearity depends on the resistor ratios

3-BIT VOLTAGE SCALING D/A CONVERTER WHICH MINIMIZES THE SWITCHES

Require time for the logic to perform



Accuracy Requirements of a Voltage Scaling D/A

Find the accuracy requirements for the voltage scaling D/A converter as a function of the number of bits N if the resistor string is a 5 micron wide polysilicon strip. If the relative accuracy is 2%, what is the largest number of bits that can be resolved to within ±0.5 LSB?

Assume that the ideal voltage to ground across k resistors is

$$V_k = \frac{kR}{2^N R} V_{REF}$$

The worst case variation in V_k is found by assuming all resistors above this point in the string are maximum and below this are minimum. Therefore,

$$V_k' = \frac{kR_{min}V_{REF}}{(2^N-k)R_{max} + kR_{min}}$$

The difference between the ideal and worst case voltages is,

$$\left|\frac{V_k}{V_{REF}} - \frac{V_k'}{V_{REF}}\right| = \left|\frac{kR}{2^N R} - \frac{kR_{min}}{(2^N-k)R_{max} + kR_{min}}\right|$$

Assuming that this difference should be less than 0.5 LSB gives,

$$\left|\frac{kR}{2^N R} - \frac{kR_{min}}{(2^N-k)R_{max} + kR_{min}}\right| < \frac{0.5}{2^N}$$

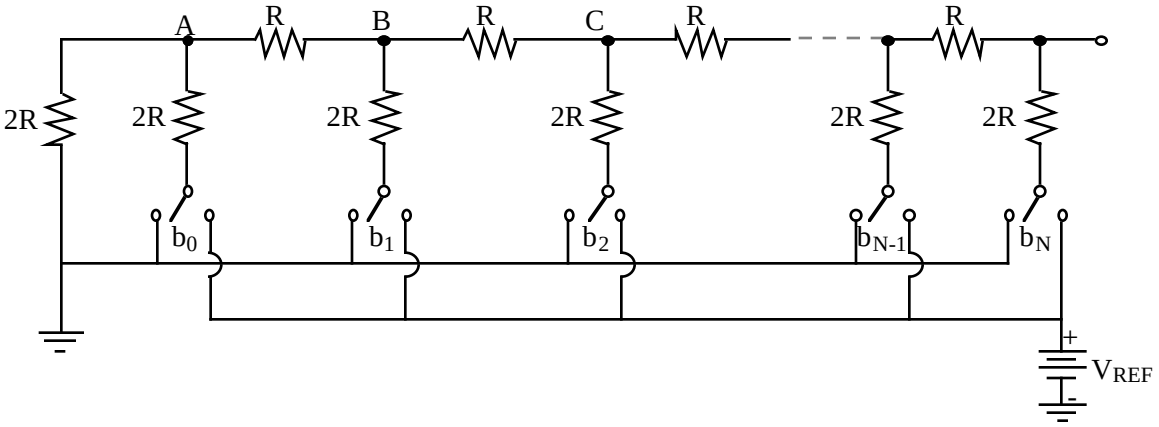
Expressing R_{max} as $R+0.5\Delta R$ and R_{min} as $R-0.5\Delta R$ and assuming the worst case occurs midway in the resistor string where $k=0.5(2^N)$ and assuming that 5 micron polysilicon has a 2% relative accuracy gives,

$$\left|0.5 - \frac{0.5(R-0.5\Delta R)}{0.5(R+0.5\Delta R) + 0.5(R-0.5\Delta R)}\right| = \left|\frac{1}{4}\frac{\Delta R}{R}\right| < \frac{1}{2}\,2^{-N}$$

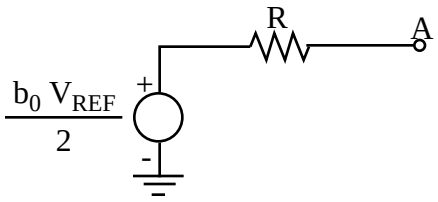
$$\Rightarrow \quad \left|\frac{\Delta R}{R} < \frac{1}{2^{N-1}}\right| \quad \text{or} \quad \left|0.25(0.02)\right| < 0.5(2^{-N}) \quad \Rightarrow \quad N = 6$$

R-2R LADDER DAC's

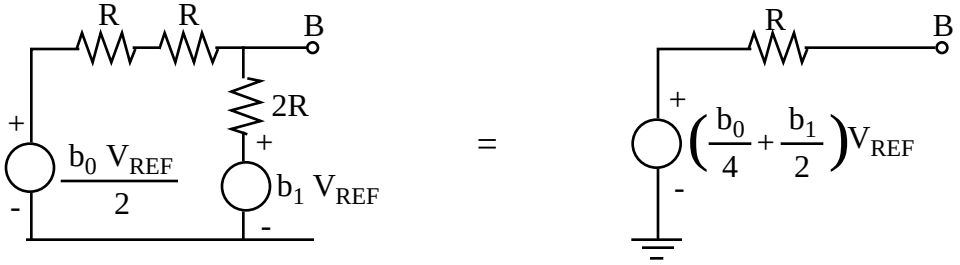
Configuration:



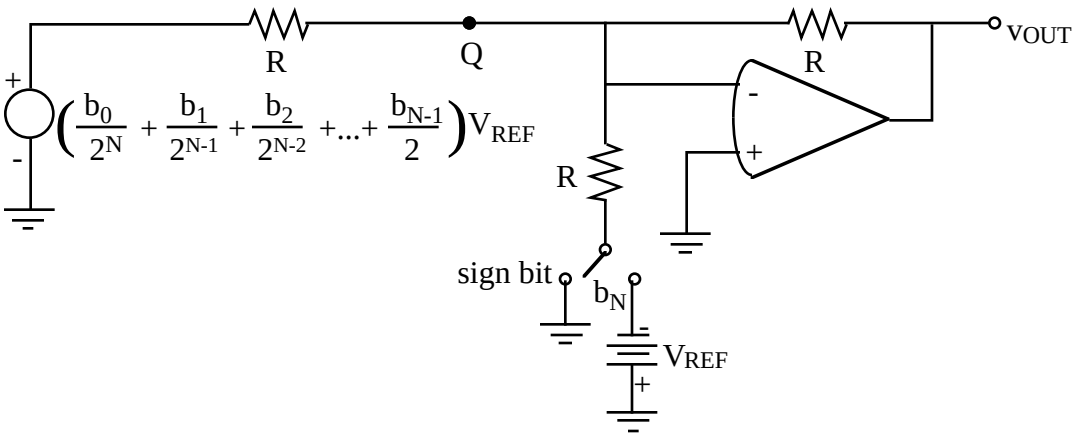
Equivalent circuit at A:



Equivalent circuit at B:

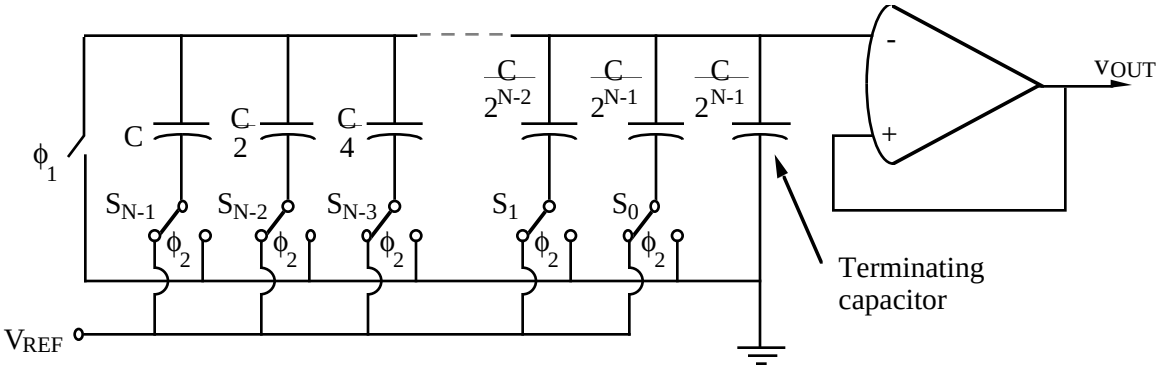


Finally, the equivalent circuit at Q:



X.3 CHARGE SCALING D/A CONVERTER

Binary weighted capacitor array:



Operation:

1.) During ϕ_1, all capacitors are discharged.

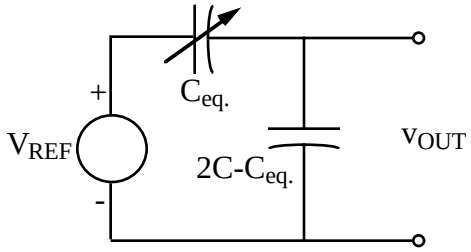
2.) During ϕ_2, capacitors with $b_i = 1$ are connected to V_{REF} and capacitors with $b_i = 0$ are grounded.

3.) The resulting output voltage is,

$$v_{OUT} = V_{REF}\left(\frac{b_{N-1}C}{2C} + \frac{b_{N-2}C/2}{2C} + \frac{b_{N-3}C/4}{2C} + \cdots + \frac{b_0 C/(2^{N-1})}{2C}\right)$$

If $C_{eq.}$ is defined as the sum of all capacitances connected to V_{REF}, then

$$v_{OUT} = \left(\frac{C_{eq.}}{2C}\right) V_{REF}$$



Other Versions of the Charge Scaling D/A Converter

Bipolar Operation:

Charge all capacitors to V_{REF}. If $b_i = 1$, connect the capacitor to ground, if $b_i = 0$, connect the capacitor to V_{REF}.

Will require an extra bit to decide whether to connect the capacitors initially to ground or to V_{REF}.

Four-Quadrant Operation:

If V_{REF} can have ±values, then a full, four quadrant DAC can be obtained.

Multiplying DAC:

If V_{REF} is an analog signal (sampled and held), then the output is the product of a digital word and an analog signal and is called a multiplying DAC (MDAC).

Influence of Capacitor Ratio Accurcy on No. of Bits

Use the data of Fig.2.4-2 to estimate the number of bits possible for a charge scaling D/A converter assuming a worst case approach and the worst conditions occur at the midscale (1 = MSB).

The ideal output of the charge scaling DA converter is,

$$\frac{v_{OUT}}{V_{REF}} = \frac{C_{eq.}}{2C}$$

The worst case output of the charge scaling DA converter is,

$$\frac{v'_{OUT}}{V_{REF}} = \frac{C_{eq.(min)}}{\left(2C - C_{eq.}\right)_{(max)} + C_{eq.(min)}}$$

The difference between the ideal output and the worst case output is,

$$\left|\frac{v_{OUT}}{V_{REF}} - \frac{v'_{OUT}}{V_{REF}}\right| = \left|\frac{1}{2} - \frac{C_{eq.(min)}}{(2C - C_{eq.})_{(max)} \pm C_{eq.(min)}}\right|$$

Assuming the worst case condition occurs at midscale, then $C_{eq.} = C$

$$\therefore \left|\frac{v_{OUT}}{V_{REF}} - \frac{v'_{OUT}}{V_{REF}}\right| = \left|\frac{1}{2} - \frac{C_{(min)}}{C_{(max)} - C_{(min)}}\right|$$

If $C_{(max)} = C + 0.5\Delta C$ and $C_{(min)} = C - 0.5\Delta C$, then setting the difference between the ideal and worst case to 0.5LSB gives,

$$\frac{0.5(C_{(max)} \pm C_{(min)}) - C_{(min)}}{C_{(max)} + C_{(min)}} \leq 0.5(1/2^N)$$

or

$$C_{(max)} - C_{(min)} \leq \frac{1}{2^N}(C_{(max)} + C_{(min)})$$

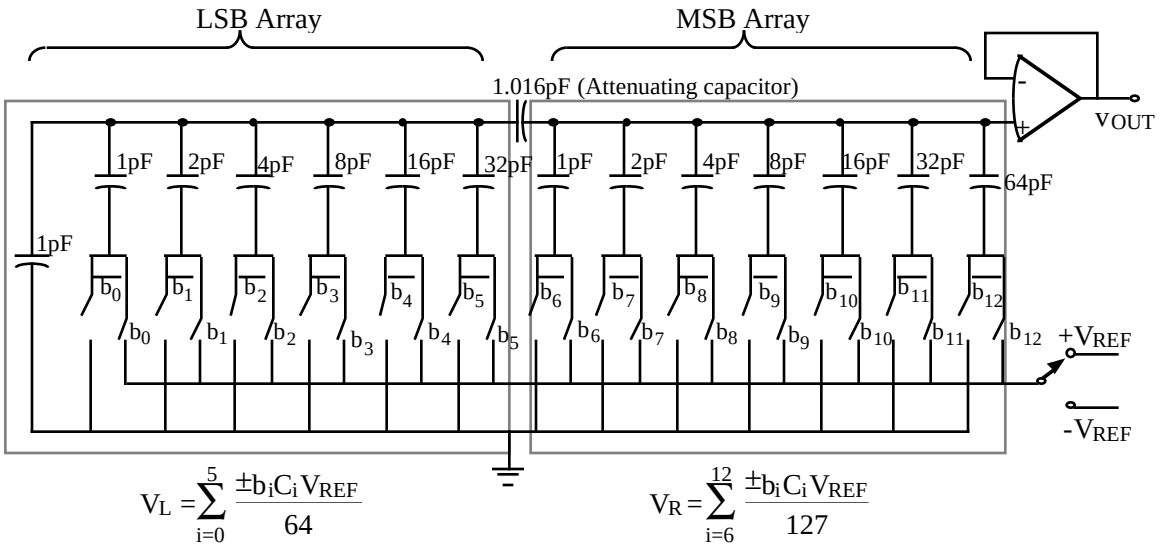
or

$$\Delta C \leq \frac{1}{2^N}\,2C \quad \Rightarrow \quad \left|\frac{\Delta C}{2C}\right| \leq 2^{-N} \Rightarrow \quad \left|\frac{\Delta C}{C}\right| \leq \frac{1}{2^{N-1}}$$

A 50μm x 50μm unit capacitor gives a relative accuracy of 0.1% and N = 11 bits. It is more appropriate that the relative accuracy is a function of N. For example, if $\Delta C/C \approx 0.001 + 0.0001N$, then N=9 bits.

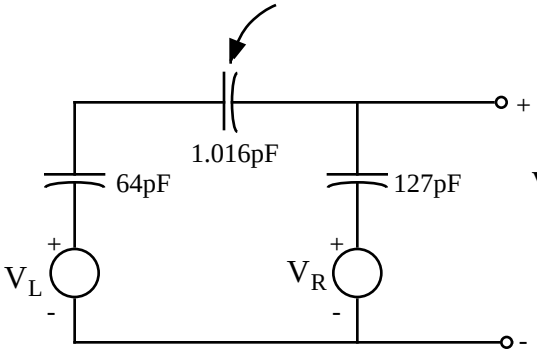
Increasing the Number of Bits for a Charge Scaling D/A Converter

Use a capacitive divider. For example, a 13-bit DAC-



An equivalent circuit-

$$\frac{1}{64} + \frac{1}{C} = 1 \Rightarrow C = \frac{64}{63} \approx 1.016$$



$$v_{OUT} = \frac{\frac{1}{64} + \frac{63}{64}}{\frac{1}{64} + \frac{63}{64} + \frac{1}{127}} V_R + \frac{\frac{1}{127}}{\frac{1}{64} + \frac{63}{64} + \frac{1}{127}} V_L$$

$$= \frac{127}{128} V_R + \frac{1}{128} V_L$$

$$V_R = \sum_{i=6}^{12} \frac{\pm b_i V_{REF} C_i}{127} \quad \text{and} \quad V_L = \sum_{i=0}^{5} \frac{\pm b_i V_{REF} C_i}{64}$$

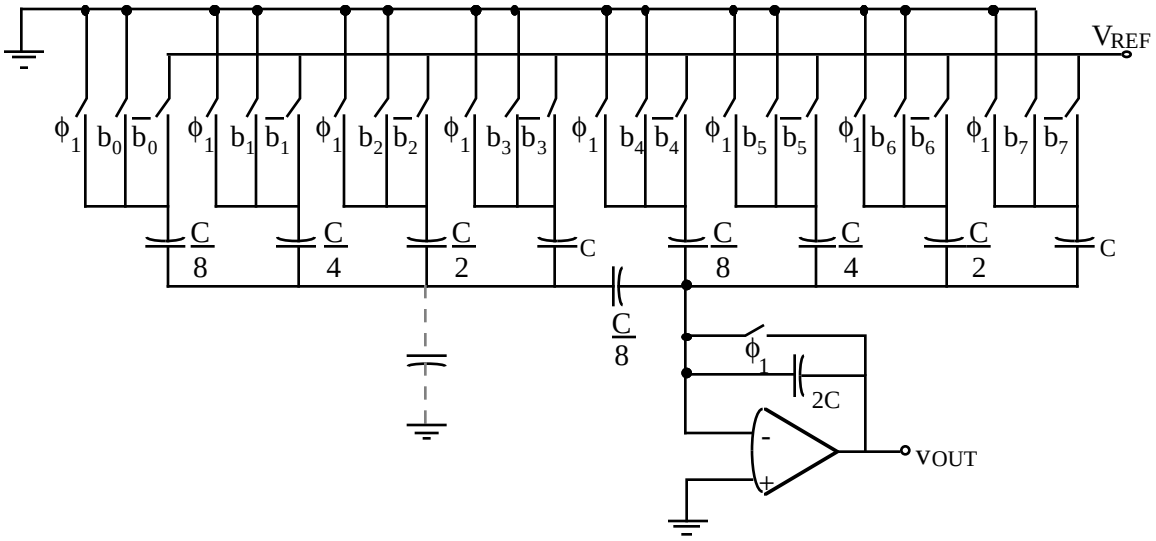
or

$$v_{OUT} = \frac{\pm V_{REF}}{128} \left[\sum_{i=6}^{12} b_i C_i + \sum_{i=0}^{5} \frac{b_i C_i}{64} \right]$$

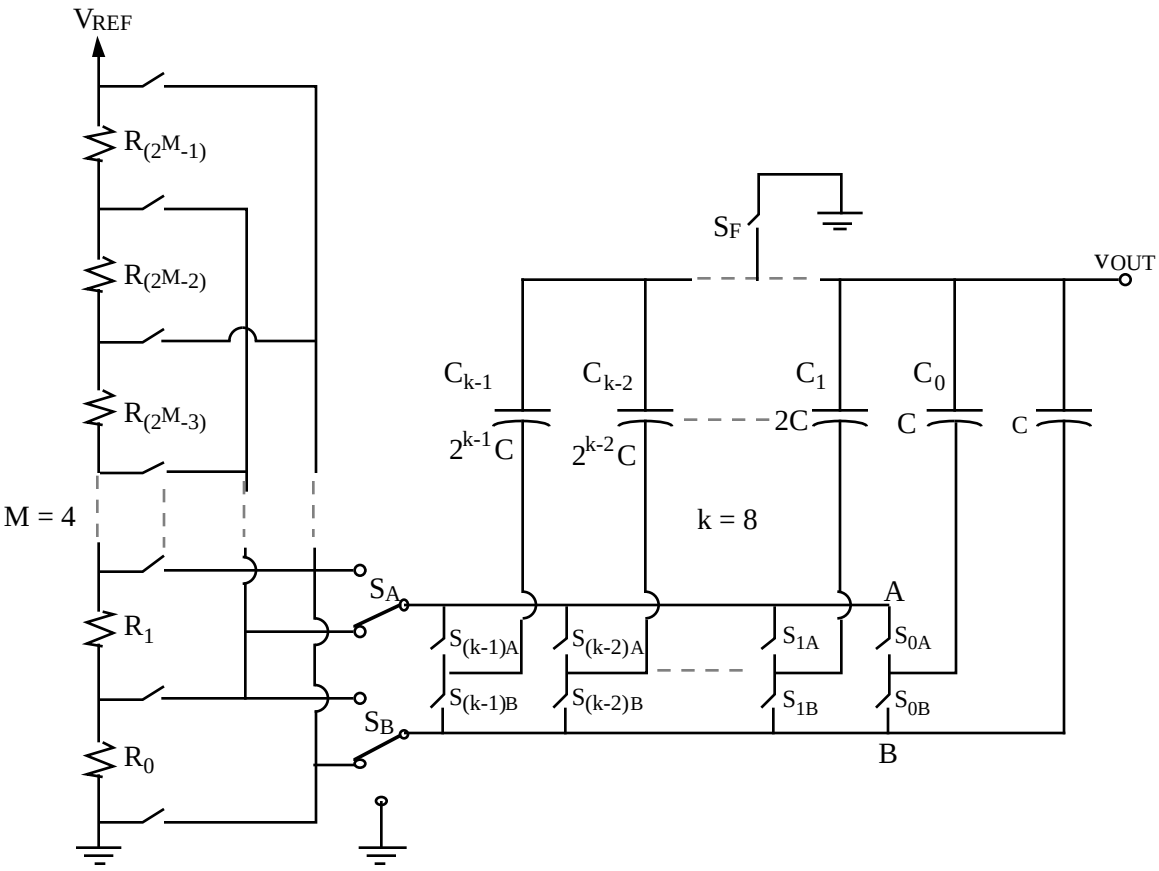
Removal of the Amplifier Input Capacitance Effects

Use the binary weighted capacitors as the input to a charge amplifier.

Example of A Two-Stage Configuration:



X.4 - VOLTAGE SCALING-CHARGE SCALING DAC'S



Advantages:

- Resistor string is inherently monotonic so the first M bits are monotonic.
- Can remove voltage threshold offsets.
- Switching both busses A and B removes switch imperfections.
- Can make tradeoffs in performance between the resistors and capacitors.
- Example with 4 MSB's voltage scaling and 8 LSB's charge scaling:

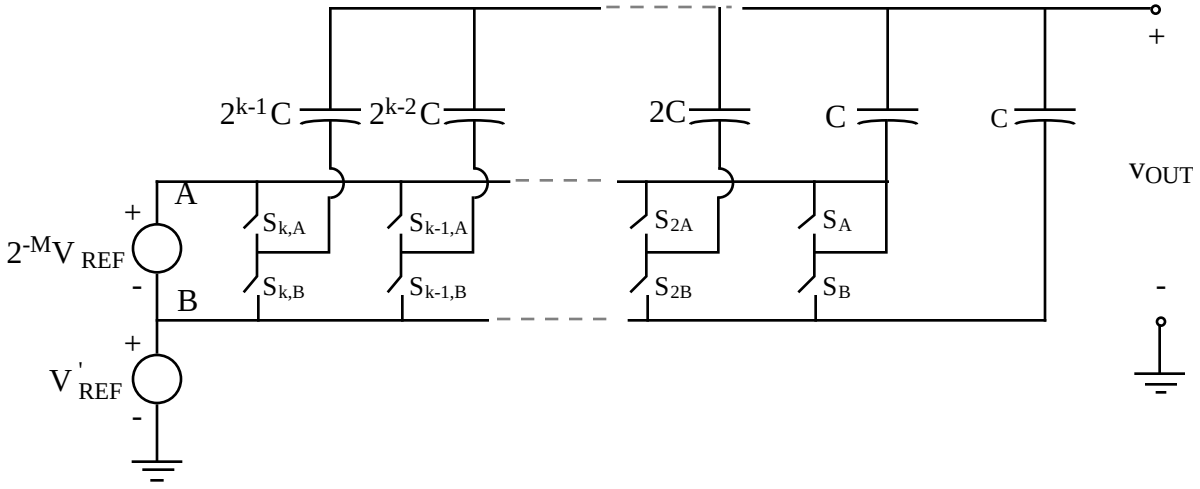
Voltage Scaling, Charge Scaling DAC - Cont'd

Operation:

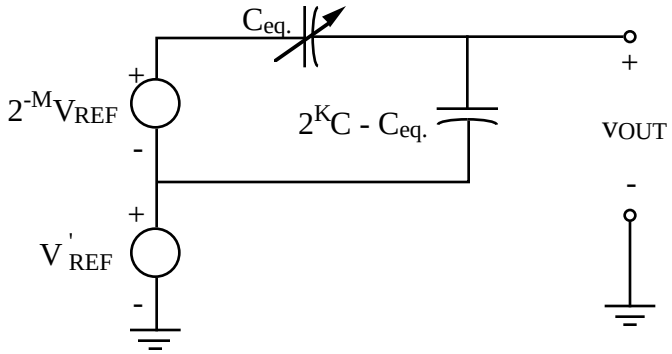
1.) S_F, S_B, and S_{1B} through $S_{k,B}$ are closed discharging all capacitors. If the output of the DAC is applied to any circuit having a nonzero threshold, switch S_B could be connected to this circuit to cancel this threshold effect.

2.) Switch S_F is opened and buses A and B are connected across the resistor whose lower and upper voltage is V'_{REF} and $V'_{REF} + 2^{-M}V_{REF}$ respectively, where

$$V'_{REF} = V_{ref}\left(\frac{b_0}{2^M} + \frac{b_1}{2^{M-1}} + \frac{b_2}{2^{M-2}} + \cdots + \frac{b_{M-1}}{2^1}\right)$$



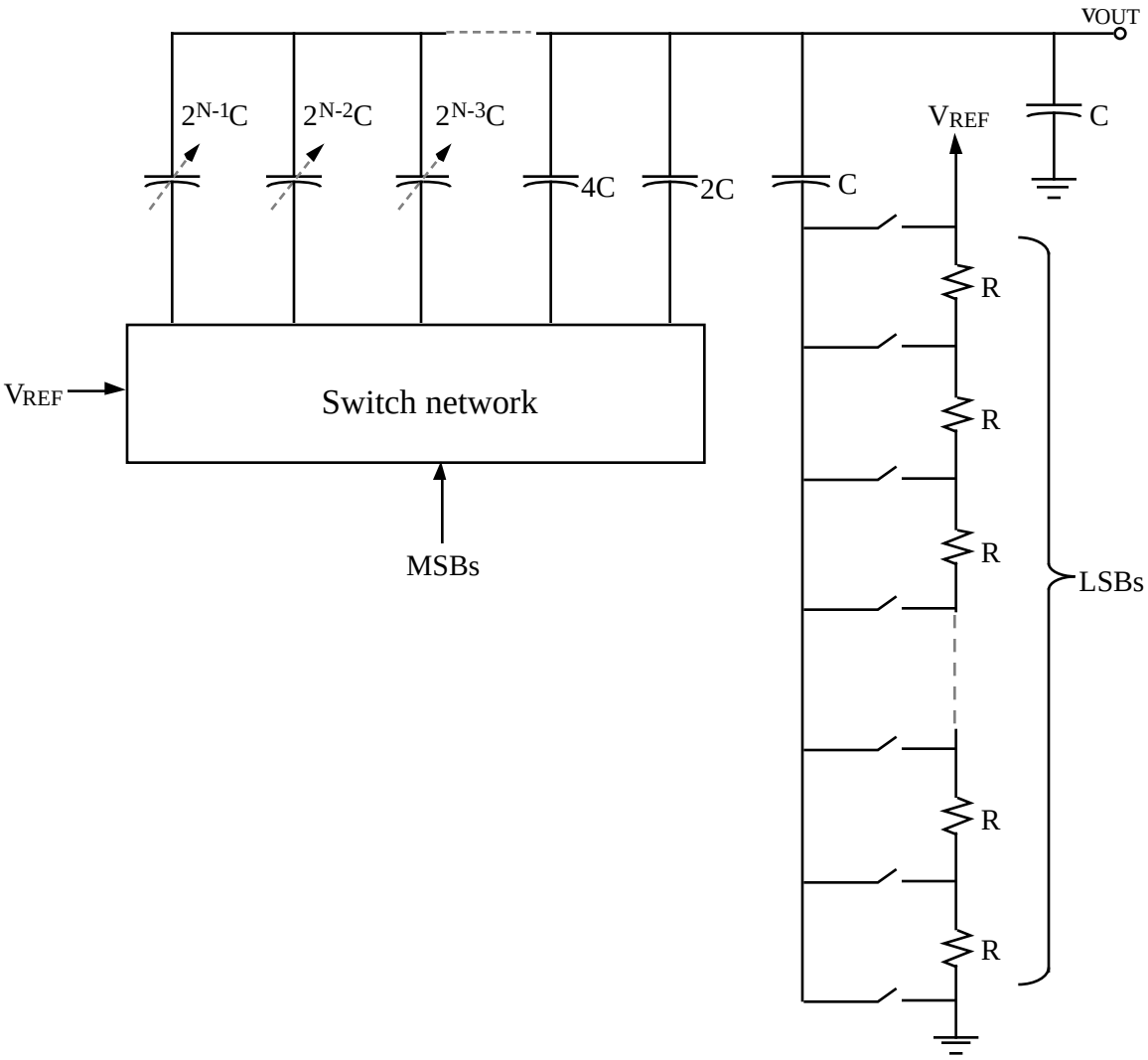
3.) Final step is to determine whether to connect the bottom plates of the capacitors to bus A (b_i=1) or bus B (b_i=0).



$$v_{OUT} = \sum_{i=0}^{M+K-1} b_i 2^{-(M+K-i)} V_{REF}$$

Charge Scaling, Voltage Scaling DAC

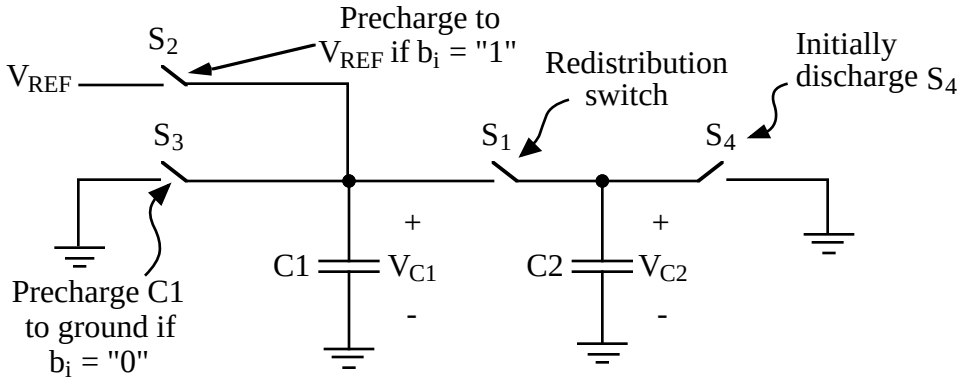
Use capacitors for MSB's and resistors for LSB's



- Resistors must be trimmed for absolute accuracy.
- LSB's are monotonic.

X.5- OTHER TYPES OF D/A CONVERTERS

CHARGE REDISTRIBUTION SERIAL DAC

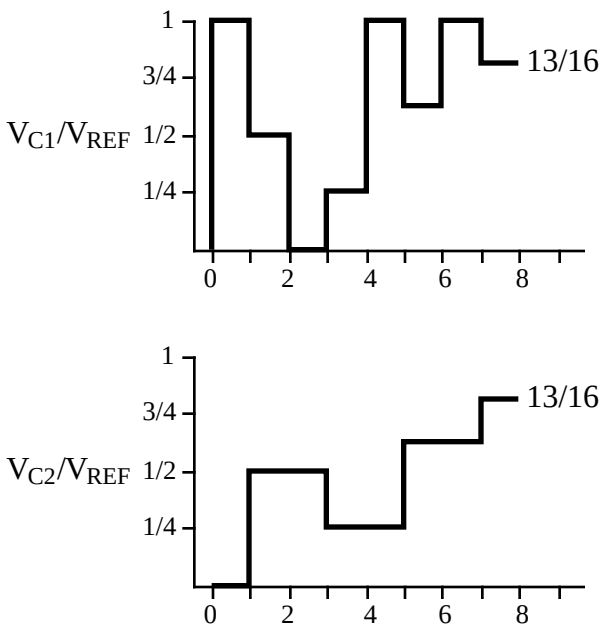


C1 = C2
b_0 = LSB
b_1 = NLSB
.
.
.
b_N = MSB

Conversion sequence:

4 Bit D/A Converter

INPUT WORD: 1101



Close S_4: $V_{C2} = 0$

Start with LSB first-

Close S_2 (b_0=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = \frac{V_{REF}}{2} = V_{C2}$

Close S_3 (b_1=0): $V_{C1} = 0$

Close S_1: $V_{C1} = V_{C2} = \frac{V_{REF}}{4}$

Close S_2 (b_2=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{5}{8} V_{REF}$

Close S_2 (b_3=1): $V_{C1} = V_{REF}$

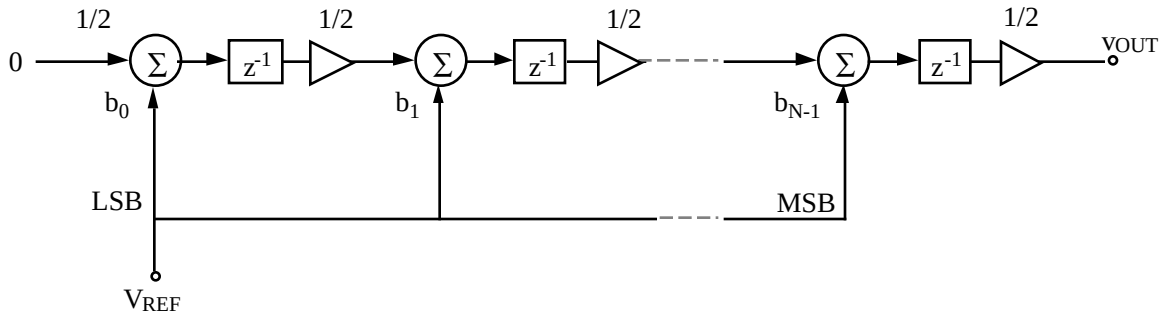
Close S_1: $V_{C1} = V_{C2} = \frac{13}{16} V_{REF}$

Comments:

- LSB must go first.
- n cycles to make an n-bit D-A conversion.
- Top plate parasitics add error.
- Switch parasitics add error.

ALGORITHMIC SERIAL DAC

Pipeline Approach to Implementing a DAC:



$$v_{OUT}(z) = \left[\frac{b_{N-1}}{2}z^{-1} + \frac{b_{N-2}}{4}z^{-2} + \ldots + \frac{b_0}{2^N}z^{-N}\right] V_{REF}$$

where $b_i = 1$ or 0

Approaches:

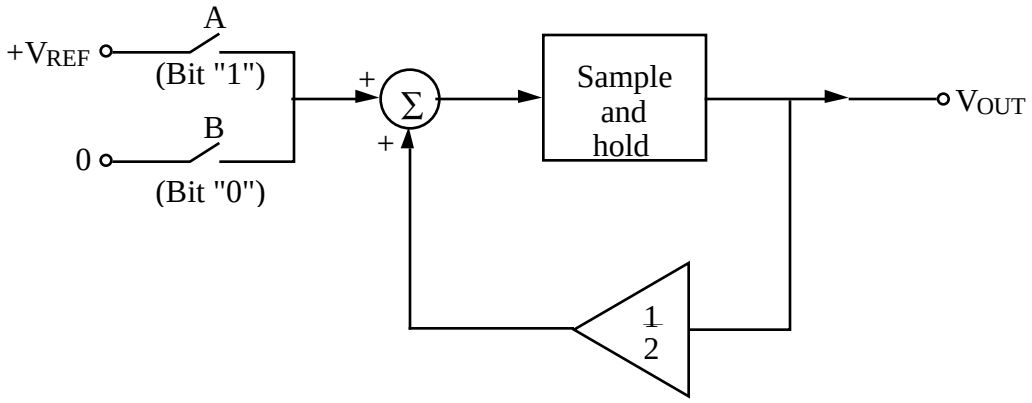
1.) Pipeline with N cascaded stages.

2.) Algorithmic.

$$v_{OUT}(z) = \frac{b_i z^{-1} V_{REF}}{1 - 0.5z^{-1}}$$

Example of an Algorithmic DAC Operation

Realization using iterative techniques:



Assume that the digital word is 11001 in the order of MSB to LSB. The steps in the conversion are:

1.) $V_{OUT}(0)$ is zeroed.

2.) LSB = 1, switch A closed,
$V_{OUT}(1) = V_{REF}$.

3.) Next LSB = 0, switch B closed,
$V_{OUT}(2) = 0 + 0.5V_{REF}$
$V_{OUT}(2) = 0.5V_{REF}$.

4.) Next LSB = 0, switch B closed,
$V_{OUT}(3) = 0 + 0.25V_{REF}$
$V_{OUT}(3) = 0.25V_{REF}$.

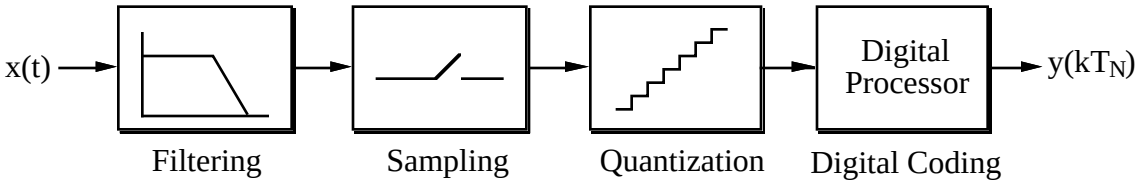
5.) Next LSB = 1, switch A closed,
$V_{OUT}(4) = V_{REF} + (1/8)V_{REF}$
$V_{OUT}(4) = (9/8)V_{REF}$.

6.) Finally, the MSB is 1,
switch A is closed, and
$V_{OUT}(5) = V_{REF} + (9/16)V_{REF}$
$V_{OUT}(5) = (25/16)V_{REF}$

7.) Finally, the MSB+1 is 0 (always last cycle),
switch A is closed, and
$V_{OUT}(6) = (25/32)V_{REF}$

X.6 - CHARACTERIZATION OF ANALOG TO DIGITAL CONVERTERS

General A/D Converter Block Diagram



A/D Converter Types

1.) Serial.

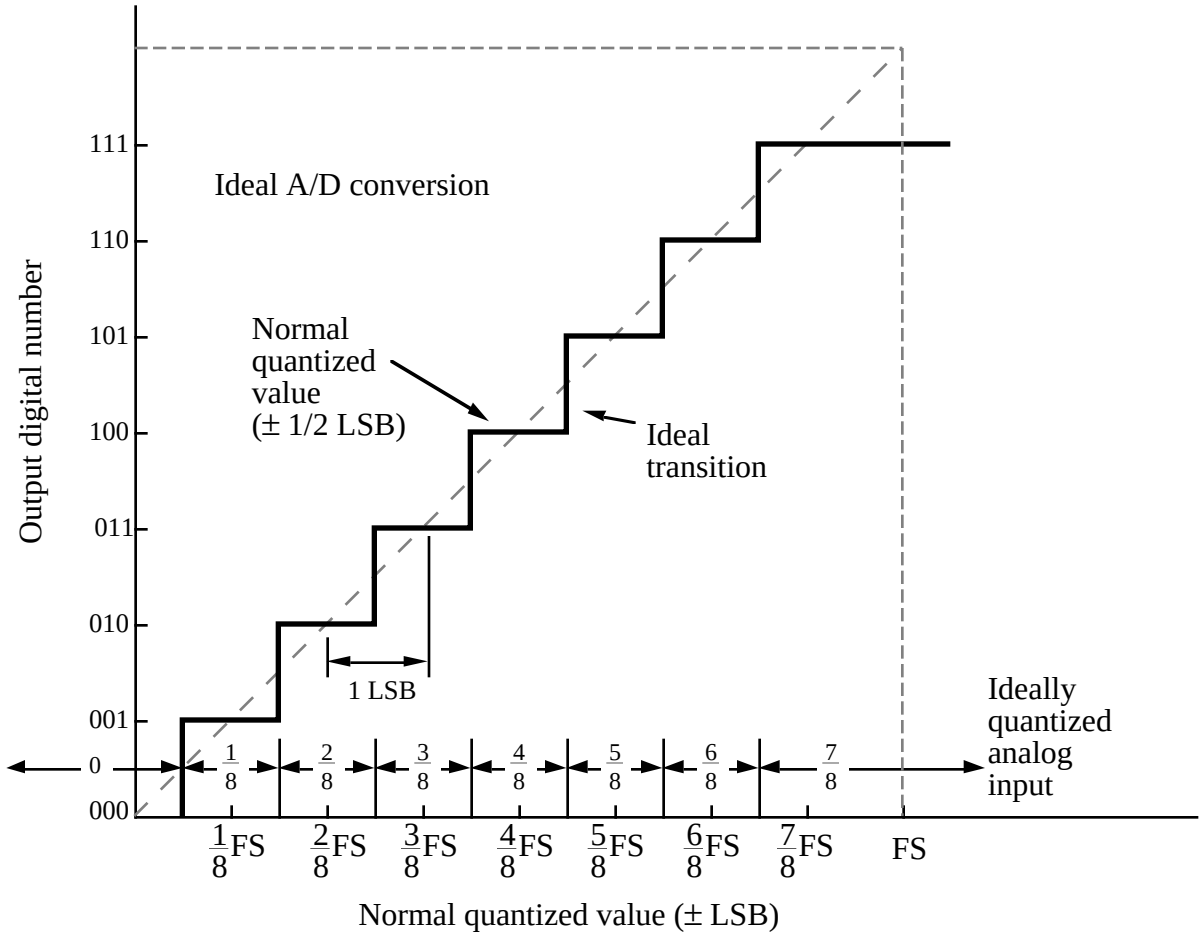
2.) Medium speed.

3.) High speed and high performance.

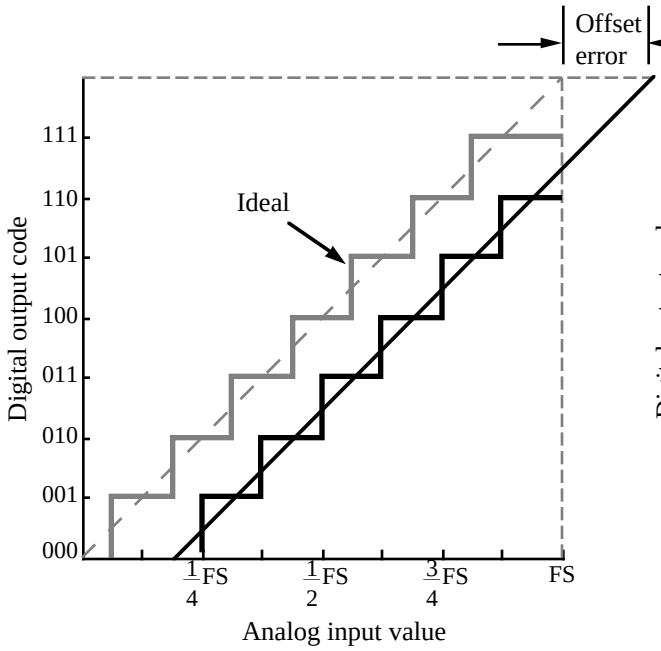
4.) New converters and techniques.

Characterization of A/D Converters

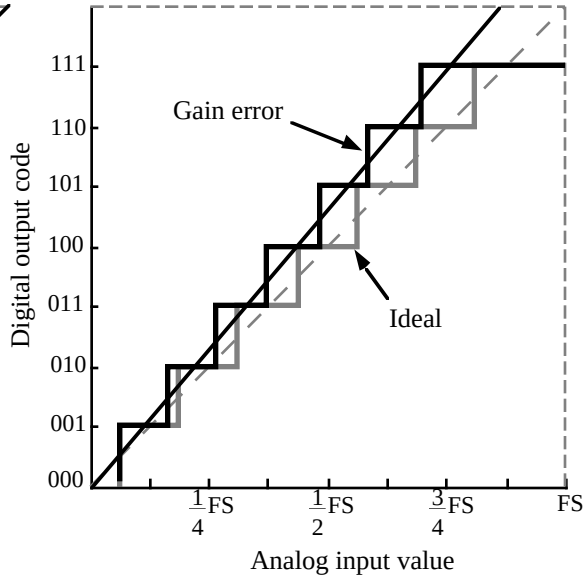
Ideal Input-Output Characteristics for a 3-bit ADC



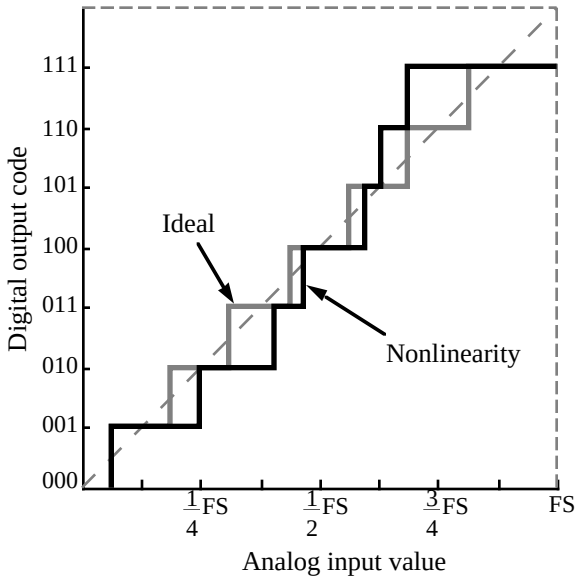
Nonideal Characteristics of A/D Converters



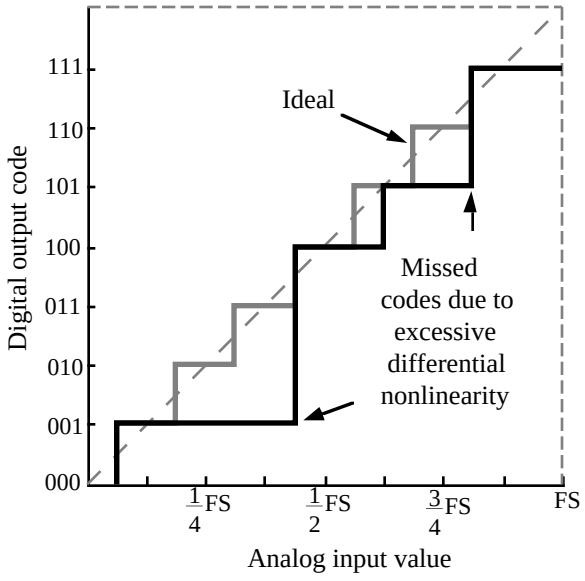
Offset Error



Scale factor (gain) error

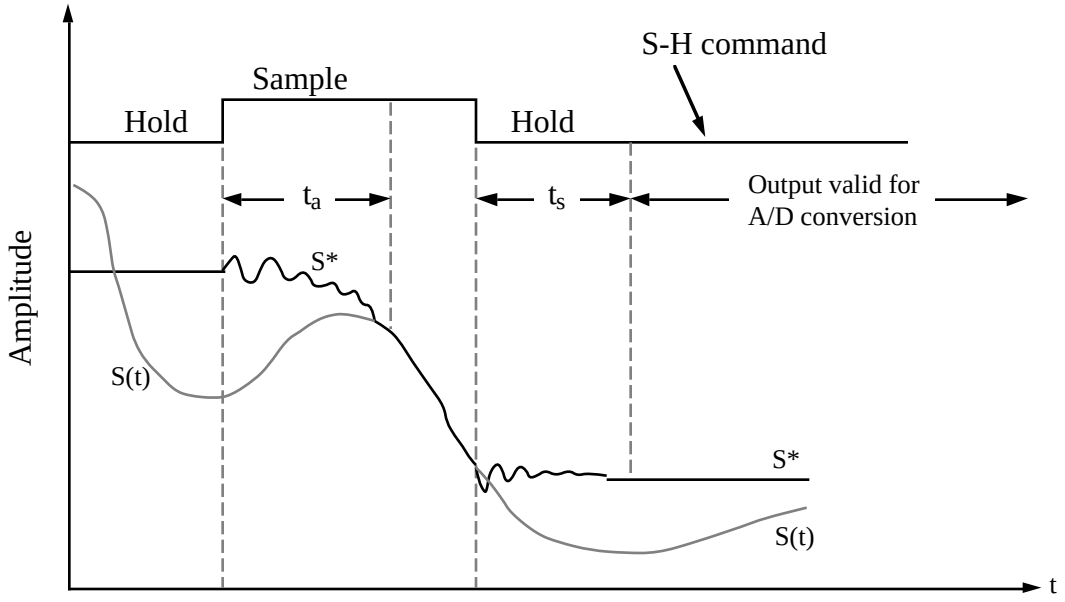


Integral Nonlinearity



Differential Nonlinearity

Sampled Data Aspect of ADC's



$T_{sample} = t_s + t_a$

t_a = acquisition time

t_s = settling time

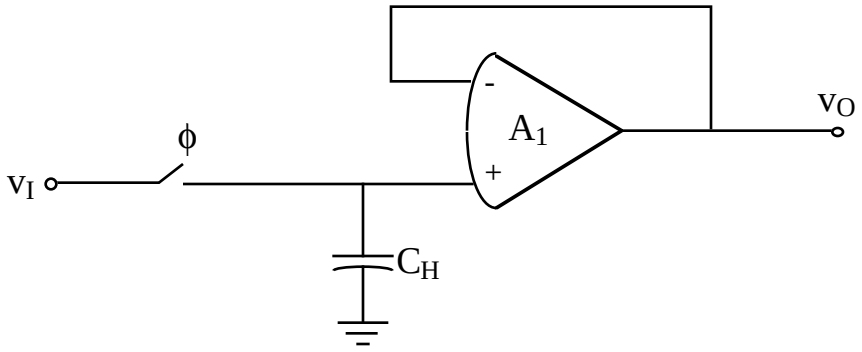
t_{ADC} = time for ADC to convert analog input to digital word.

Conversion time = $t_s + t_a + t_{ADC}$.

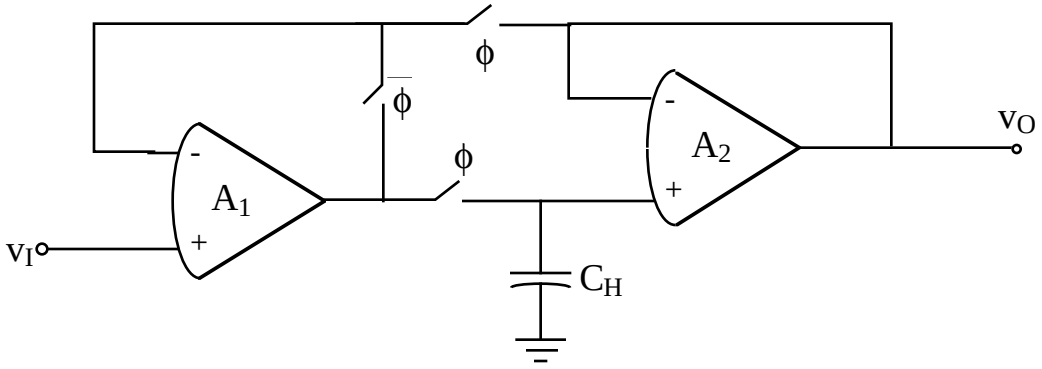
Noise = $\frac{kT}{C}$ V^2 (rms)

Sample and Hold Circuits

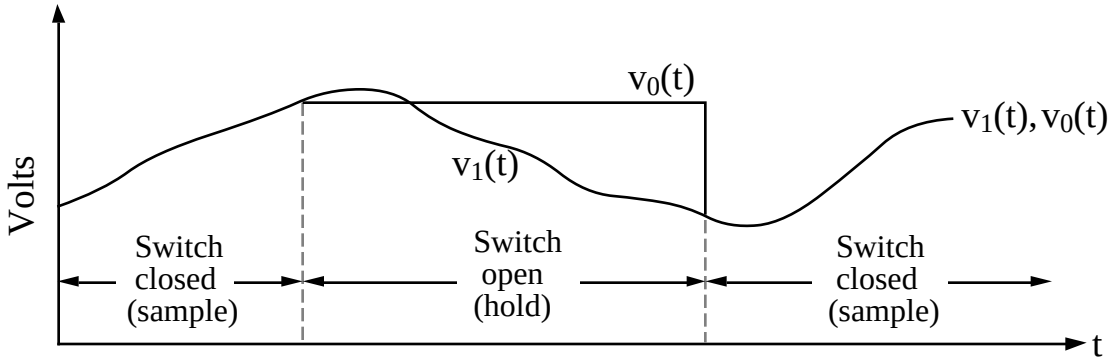
Simple



Improved

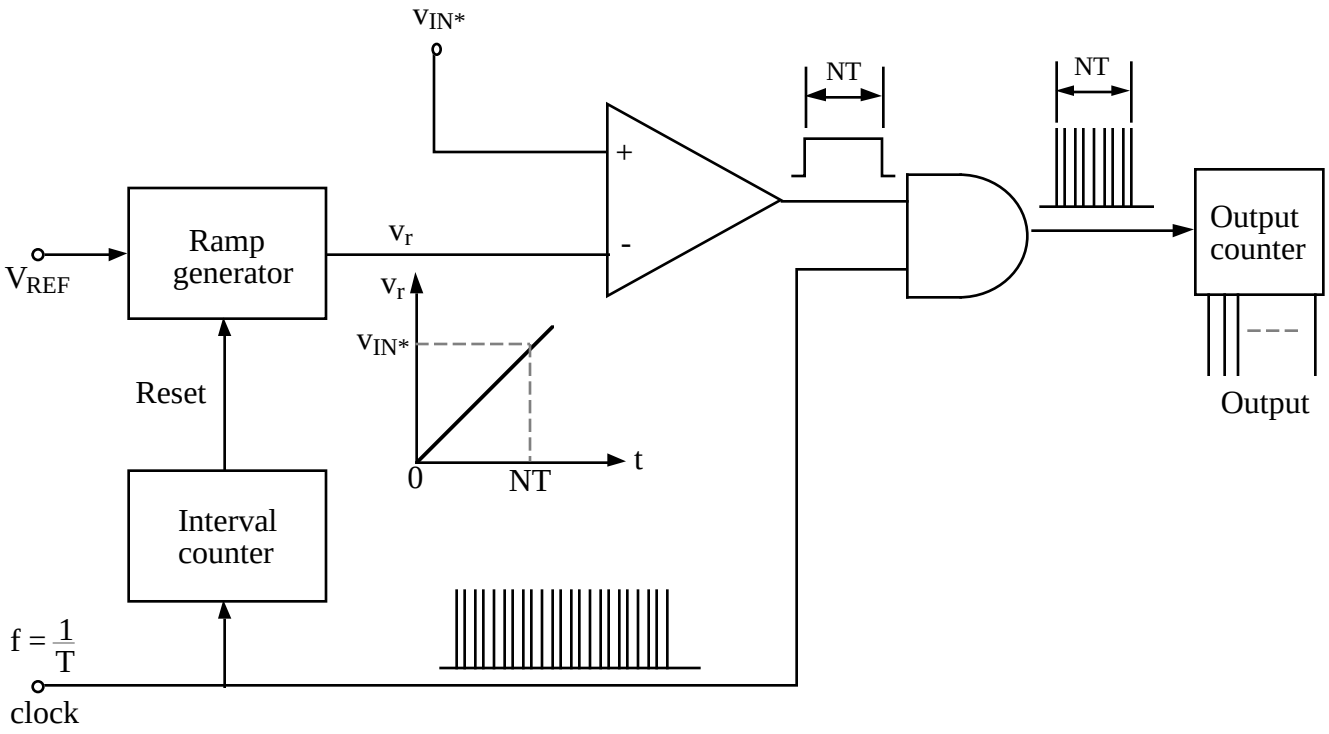


Waveforms



X.7 - SERIAL A/D CONVERTERS

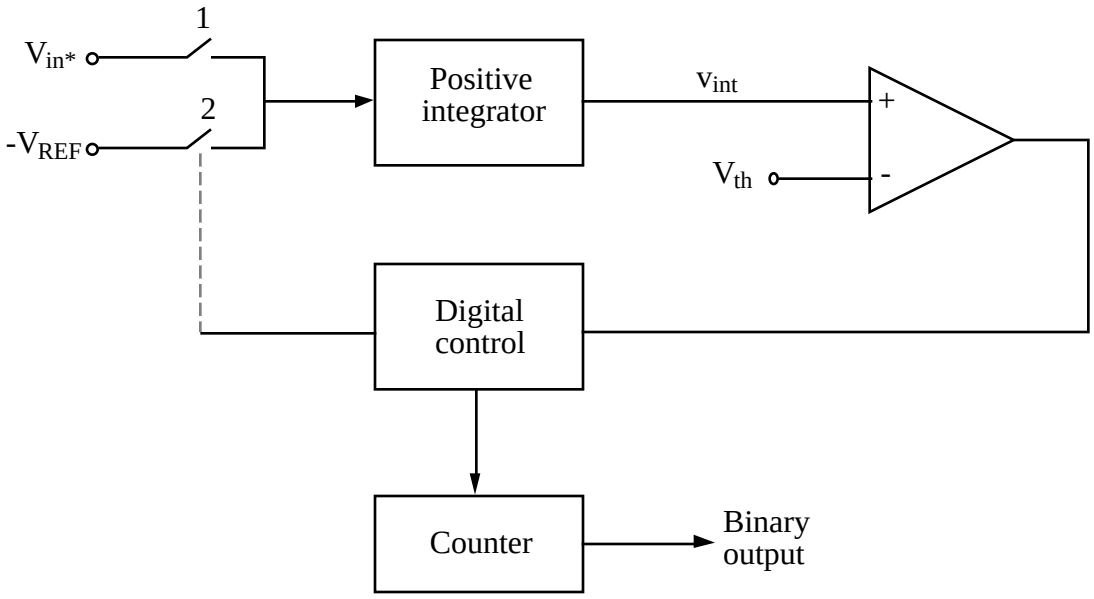
Single-Slope, A/D Converter



- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion times

Dual Slope, A/D Converter

Block Diagram:



Operation:

1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($V_{in}^* > 0$).

2.) Reset by integrating until $v_{int}(0) = V_{th}$.

3.) Integrate V_{in}^* for N_{ref} clock cycles to get,

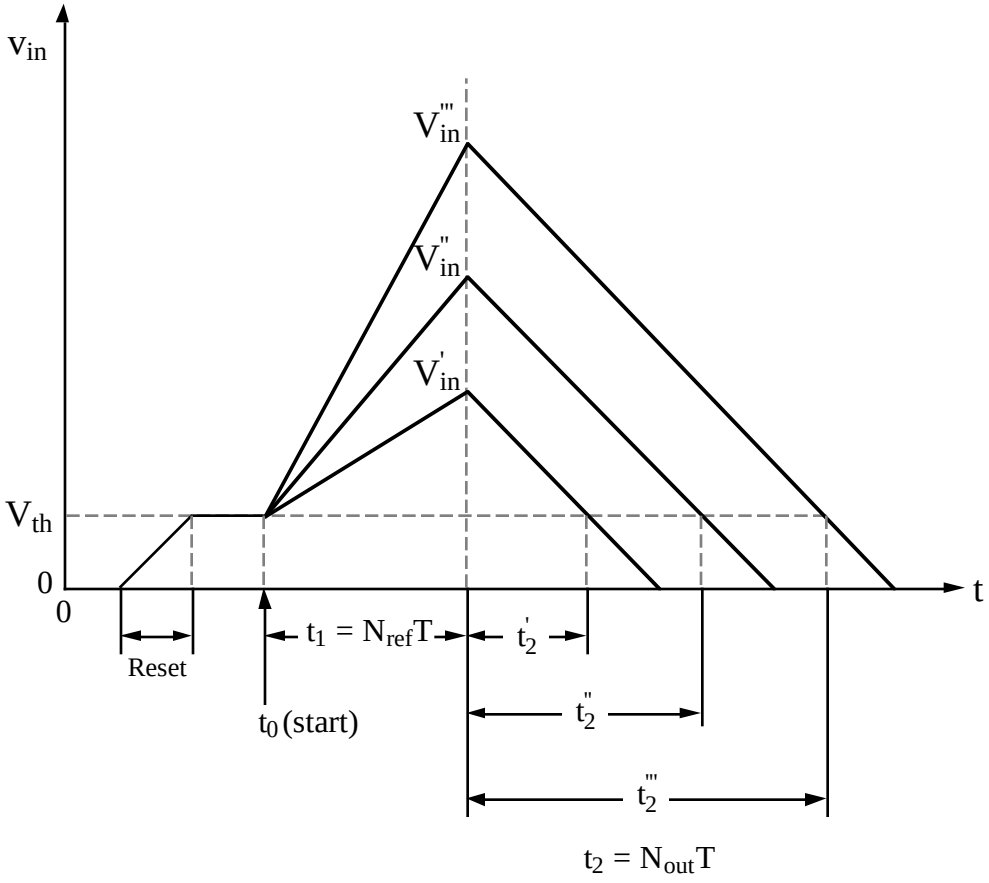
$$v_{int}(t_1) = v_{int}(N_{ref}T) = k\int_0^{N_{ref}T} V_{in}^* dt + v_{int}(0) = kN_{ref}TV_{in}^* + V_{th}$$

4.) The Carry Output on the counter is used to switch the integrator from V_{in}^* to $-V_{REF}$. Integrate until v_{int} is equal to V_{th} resulting in

$$v_{int}(t_1 + t_2) = v_{int}(t_1) + k\int_{t_1}^{N_{out}T + t_1} -V_{REF}dt = V_{th}$$

$$\therefore kN_{ref}TV_{in}^* + V_{th} - kV_{REF}N_{out}T = V_{th} \Rightarrow \boxed{V_{REF}\frac{N_{out}}{N_{ref}} = V_{in}^*}$$

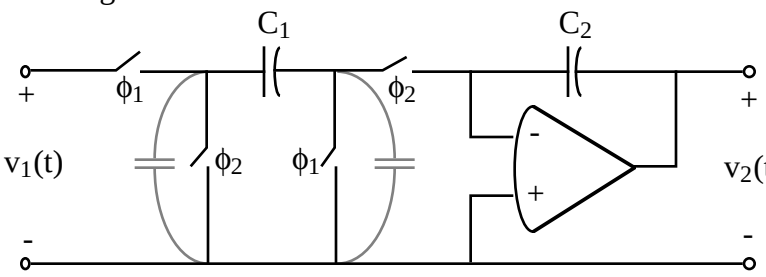
Waveform of the Dual -Slope A/D Converter



- Very accurate method of A/D conversion.
- Requires a long time -$2(2^N)T$

Switched Capacitor Integrators

Noninverting:



$f_{signal} << f_{clock}$

Operation:

Assume non-overlapping clocks ϕ_1 and ϕ_2. During ϕ_1, C_1 is charged to $v_1[(n-1)T]$ giving a charge of $q_1[(n-1)T]$ on C_1. During ϕ_2, the charge across C_1 is added to the charge already on C_2 which is $q_2[(n-1)T]$ resulting in a new charge across C_2 designated as $q_2(nT)$. The charge equation can be written as,

$$q_2(nT) = q_2[(n-1)T] + q_1[(n-1)T]$$

or

$$C_2 v_2(nT) = C_2\, v_2[(n-1)T] + C_1\, v_1[(n-1)T]$$

Using z-domain notation gives

$$C_2 v_2(z) = C_2 z^{-1} v_2(z) + C_1 z^{-1} v_1(z)$$

or

$$H(z) = \frac{v_2(z)}{v_1(z)} = \frac{C_1}{C_2}\left[\frac{z^{-1}}{1 - z^{-1}}\right]$$

Replacing z by $e^{j\omega T}$ gives,

$$H(e^{j\omega T}) = \frac{C_1}{C_2}\left[\frac{e^{-j\omega T}}{1 - e^{-j\omega T}}\right] = \frac{C_1}{C_2}\left[\frac{e^{-j\omega\frac{T}{2}}}{e^{j\omega\frac{T}{2}} - e^{-j\omega\frac{T}{2}}}\right]$$

$$= \frac{\omega_o}{j\omega}\underbrace{\left[\frac{(\omega T/2)}{\sin(\omega T/2)}\right]}_{\text{Mag. error}}\underbrace{\exp(-j\omega T/2)}_{\text{Phase error}} \approx \frac{\omega_o}{j\omega} \quad \text{if } f << f_c = \frac{1}{T}$$

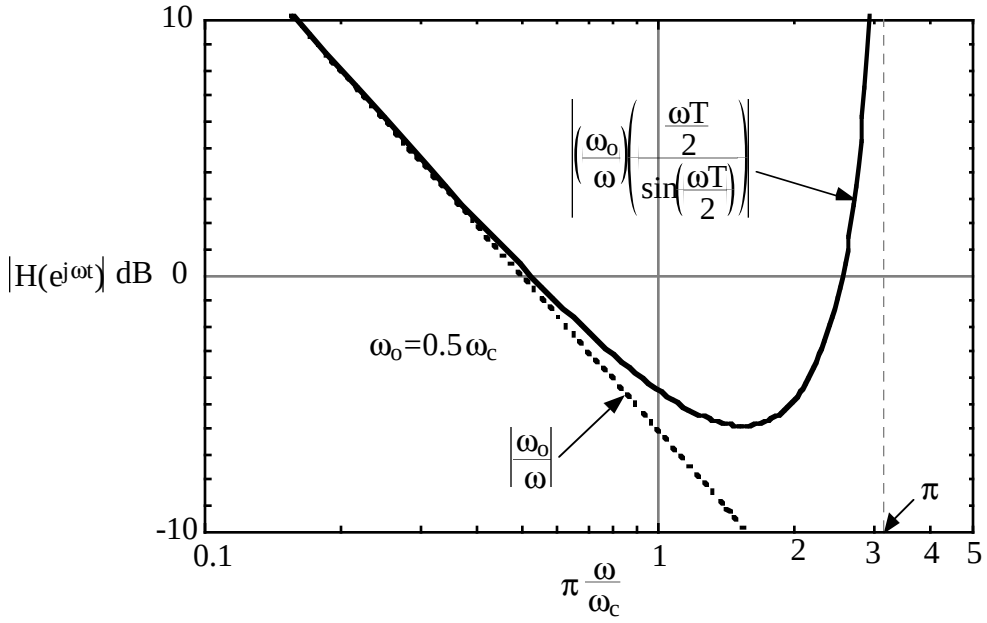
where $\omega_o = C_1/(TC_2)$, $\sin x = \frac{e^{jx} - e^{-jx}}{2j}$

Magnitude Plots of the Switched Capacitor Integrator

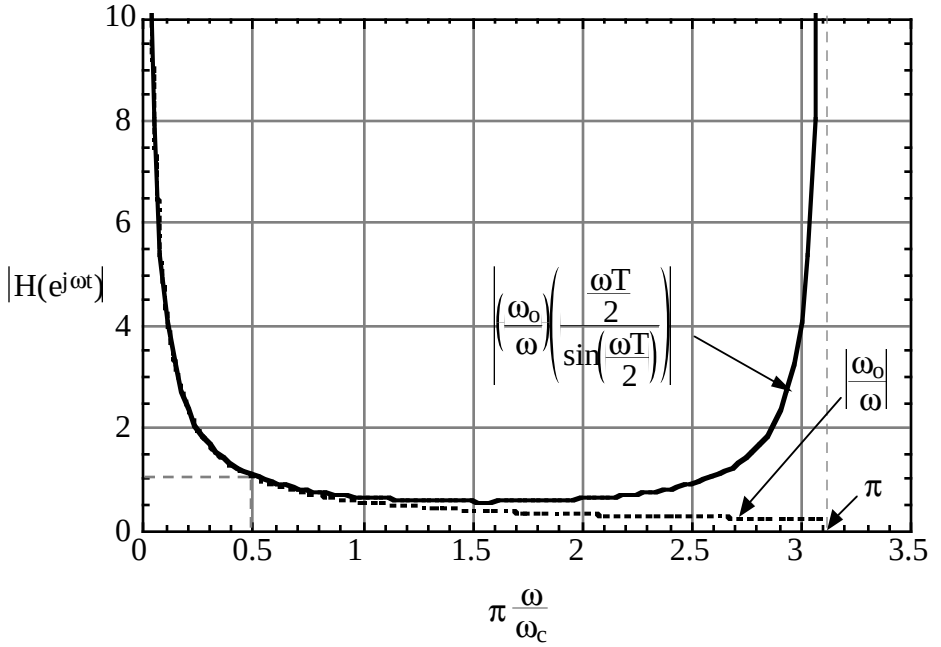
$$\omega_O = \frac{\omega_C}{2\pi}$$

$$\frac{\omega T}{2} = \frac{2\pi f}{2f_C} = \frac{\pi f}{f_C} = \frac{\pi\omega}{\omega_C}$$

Log Plot-

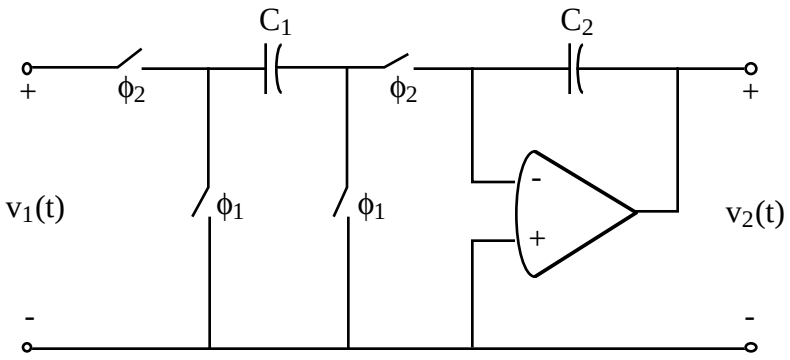


Linear Plot-



Switched Capacitor Integrators - Cont'd

Inverting:

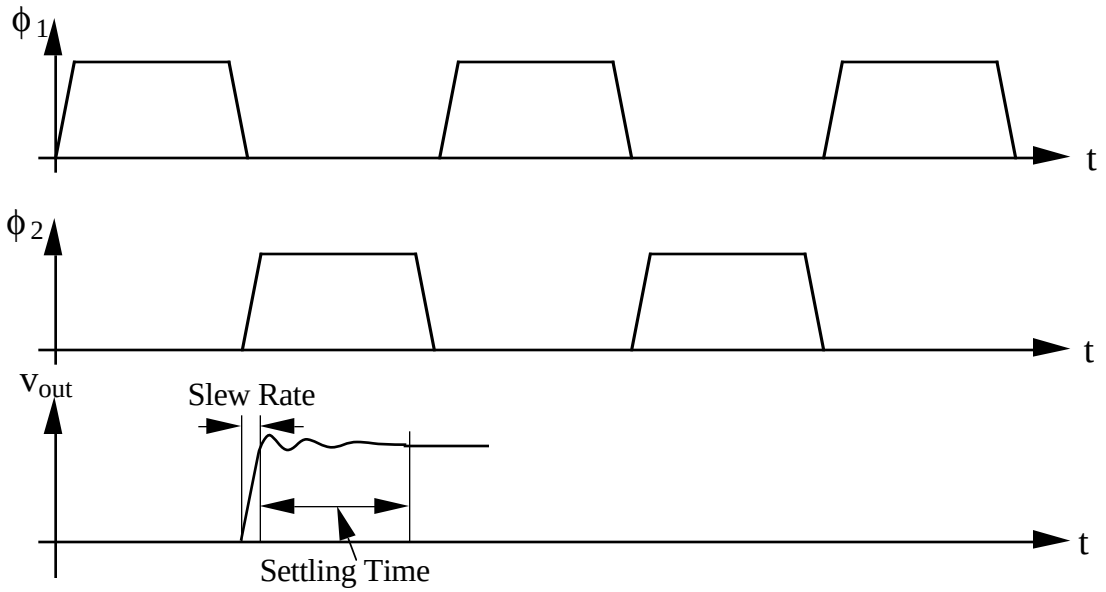


By a similar analysis, one can show that

$$H(e^{j\omega T}) \approx -\frac{\omega_o}{j\omega}\ ,\ \text{if } f << f_c = 1/T$$

Settling Time and Slew Rate of the Op Amp

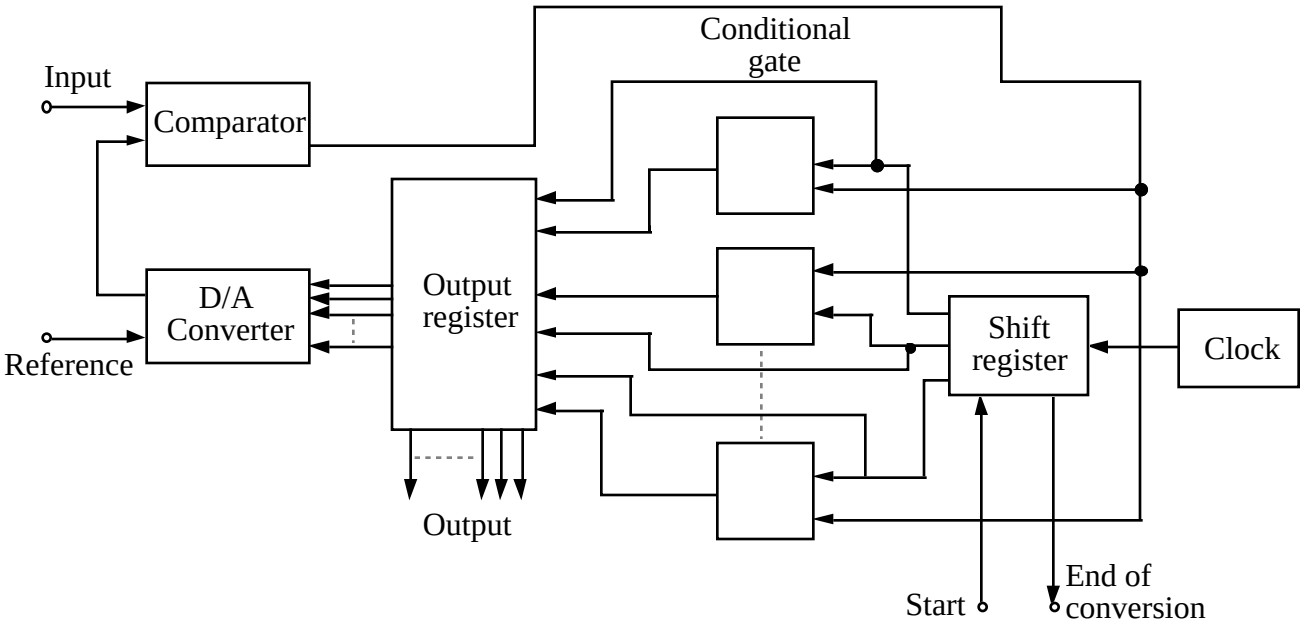
Important when the op amp plus feedback circuit has two or more poles or the op amp has a second pole.



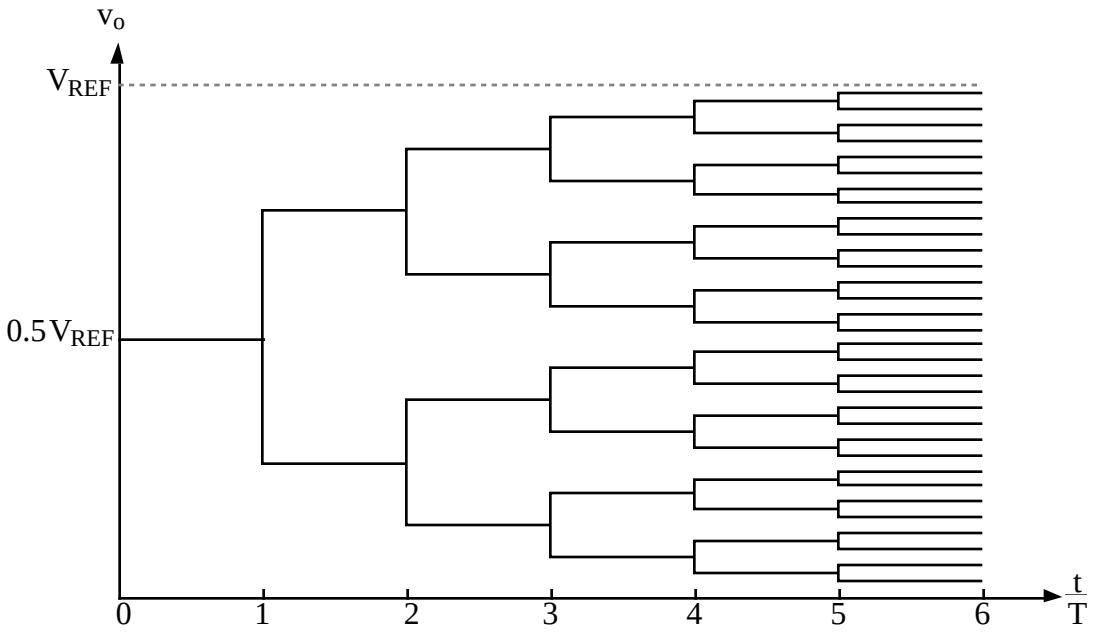
X.8 - MEDIUM SPEED A/D CONVERTERS

Conversion Time ≈ NT

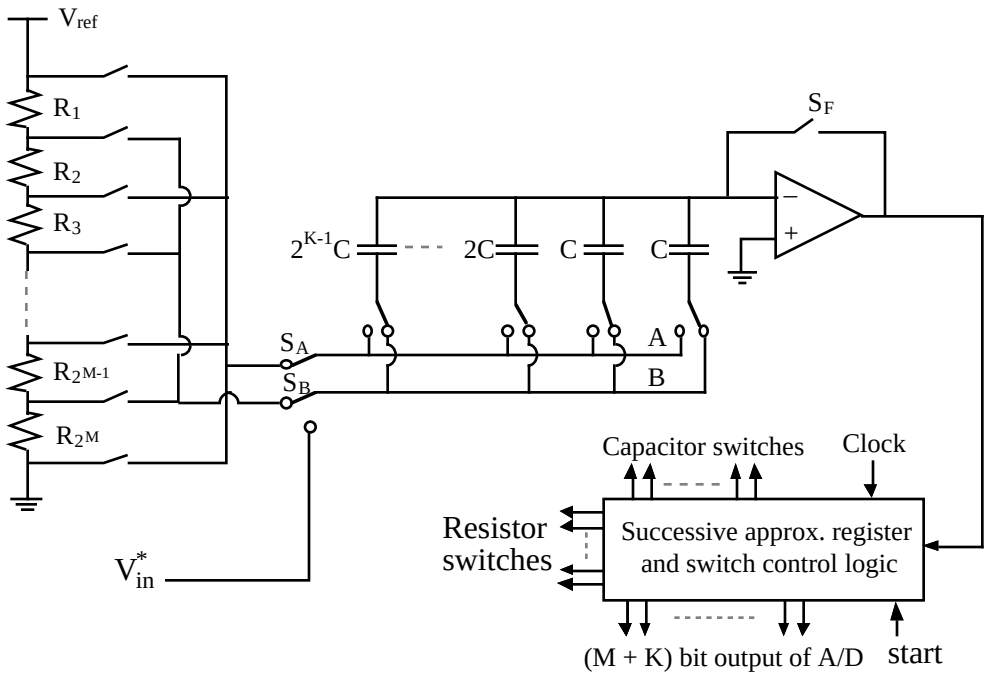
Successive ApproximationArchitecture:



Successive Approximation Process:



A Voltage-Charge Scaling Successive Approximation ADC



Operation:

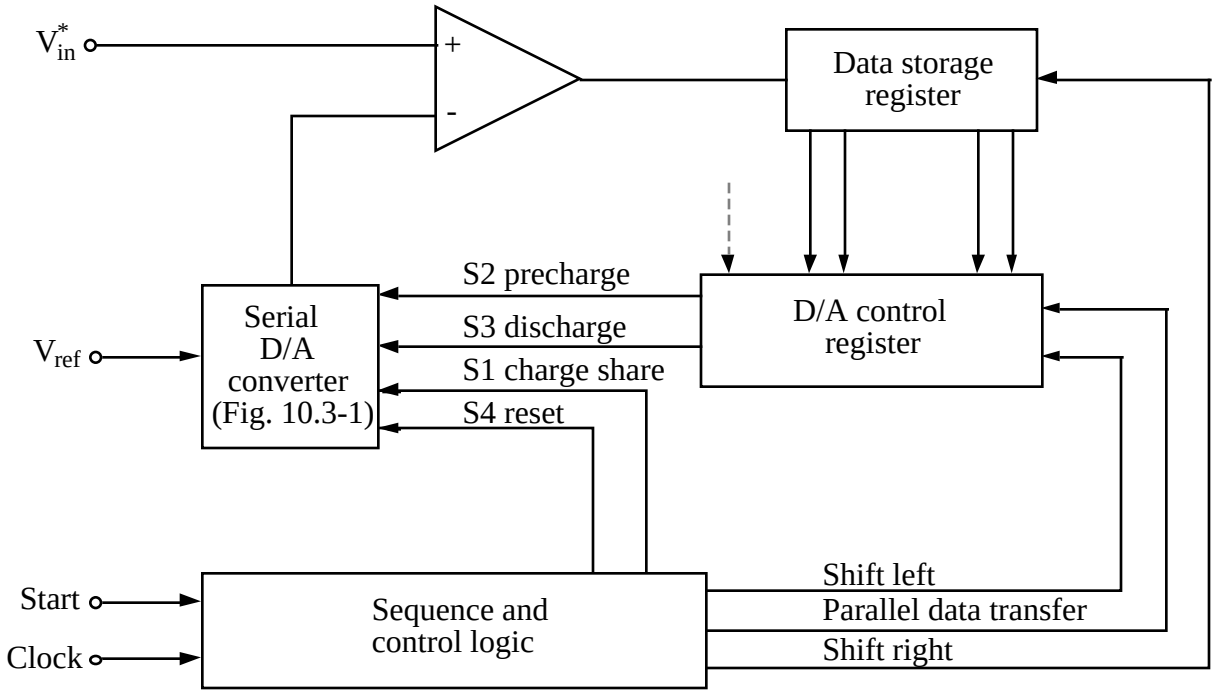
1.) With S_F closed, the bottom plates of all capacitors are connected through switch S_B to Vin^*. (Automatically accounts for voltage offsets).

2.) After S_F is opened, a successive approximation search among the resistor string taps to find the resistor segment in which the stored sample lies.

3.) Buses A and B are then connected across this segment and the capacitor bottom plates are switched in a successive approximation sequence until the comparator input voltage converges back to the threshold voltage.

Capable of 12-bit monotonic conversion with a DL of ±0.5LSB within 50μs.

A Successive Approximation ADC using a Serial DAC



Conversion Sequence:

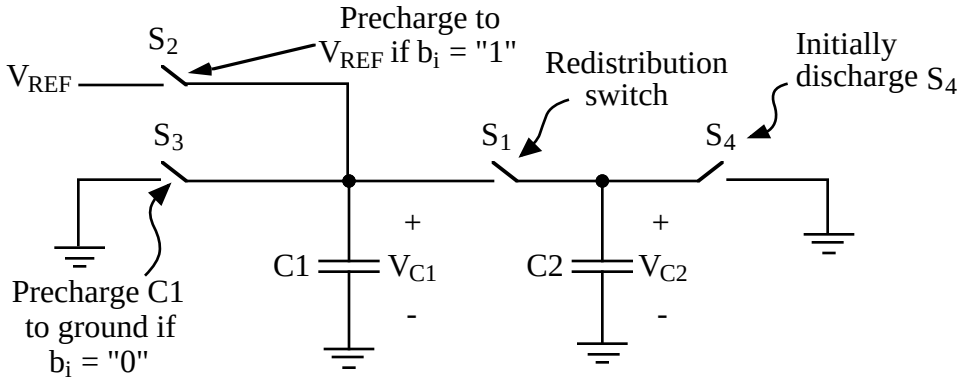
1.) Assume first K MSB's have been decided so that,

$$\text{Digital word} = a_M\frac{1}{2^N} + a_{N-1}\frac{1}{2^{N-1}} + \ldots + a_{N-K+1}\frac{1}{2^{N-K+1}} + .$$

2.) Assume (K + 1)th MSB is 1 and compare this analog output with V_{in}^* to determine a_{N-K}.

3.) Store a_{N-K} in the DATA storage register and contiune.

CHARGE REDISTRIBUTION SERIAL DAC

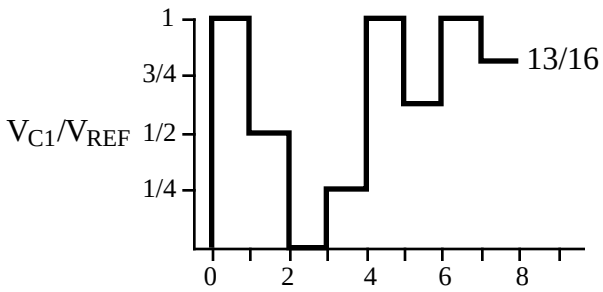


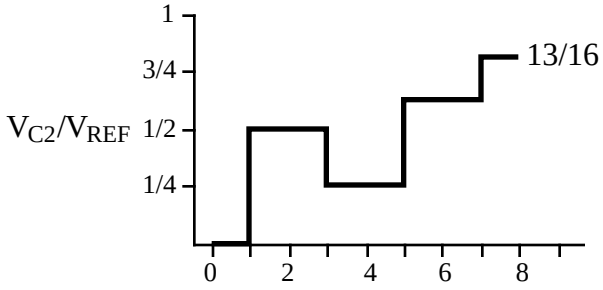
C1 = C2
b_0 = LSB
b_1 = NLSB
.
.
.
b_N = MSB

Conversion sequence:

4 Bit D/A Converter

INPUT WORD: 1101





Close S_4: $V_{C2} = 0$

Store with LSB first-

Close S_2 (b_0=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = \frac{V_{REF}}{2} = V_{C2}$

Close S_3 (b_1=0): $V_{C1} = 0$

Close S_1: $V_{C1} = V_{C2} = \frac{V_{REF}}{4}$

Close S_2 (b_2=1): $V_{C1} = V_{REF}$

Close S_1: $V_{C1} = V_{C2} = \frac{5}{8} V_{REF}$

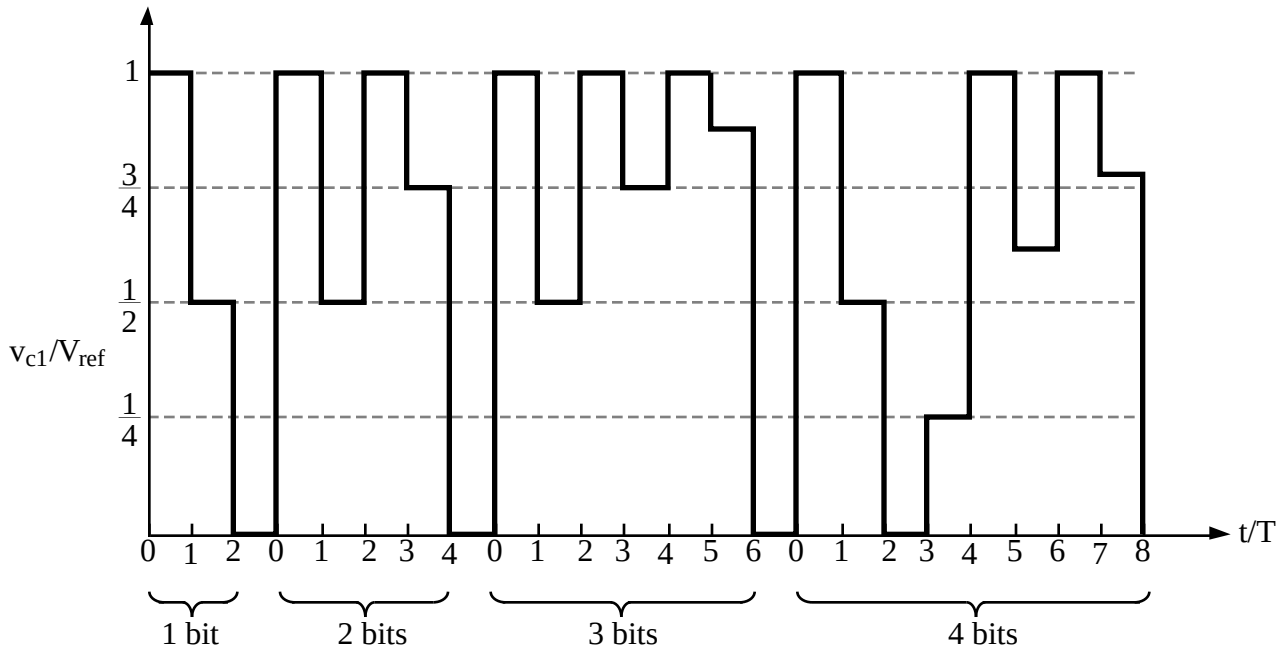
Close S_2 (b_3=1): $V_{C1} = V_{REF}$

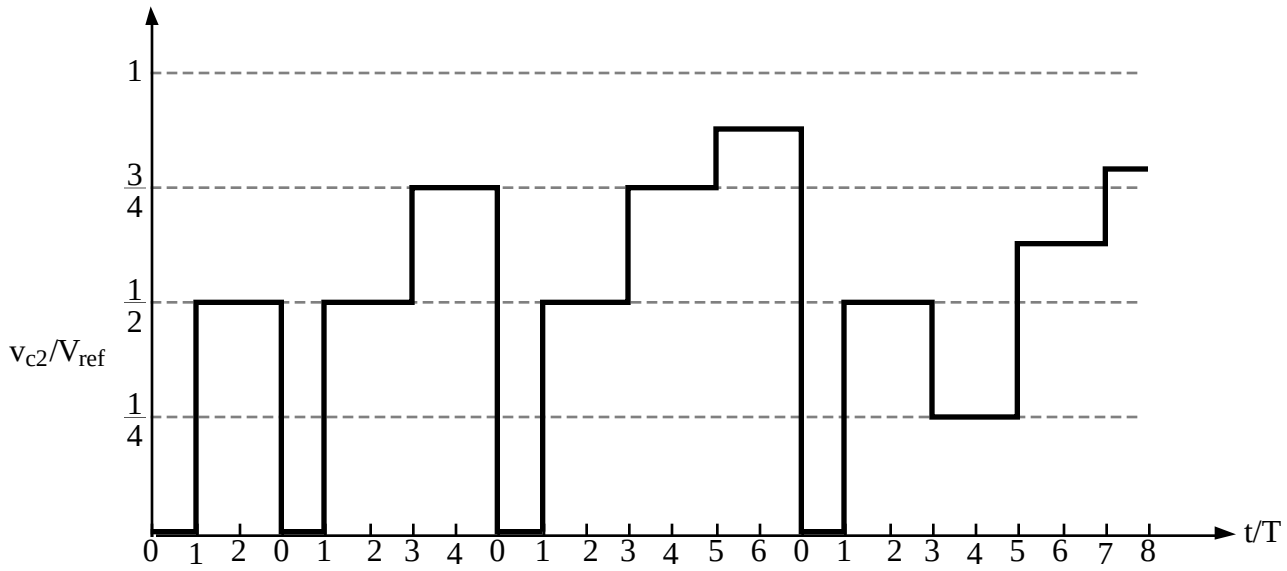
Close S_1: $V_{C1} = V_{C2} = \frac{13}{16} V_{REF}$

Comments:

- LSB must go first.
- n cycles to make an n-bit D-A conversion.
- Top plate parasitics add error.
- Switch parasitics add error.

Serial ADC Waveform for an Input of ($13/16V_{ref}$)



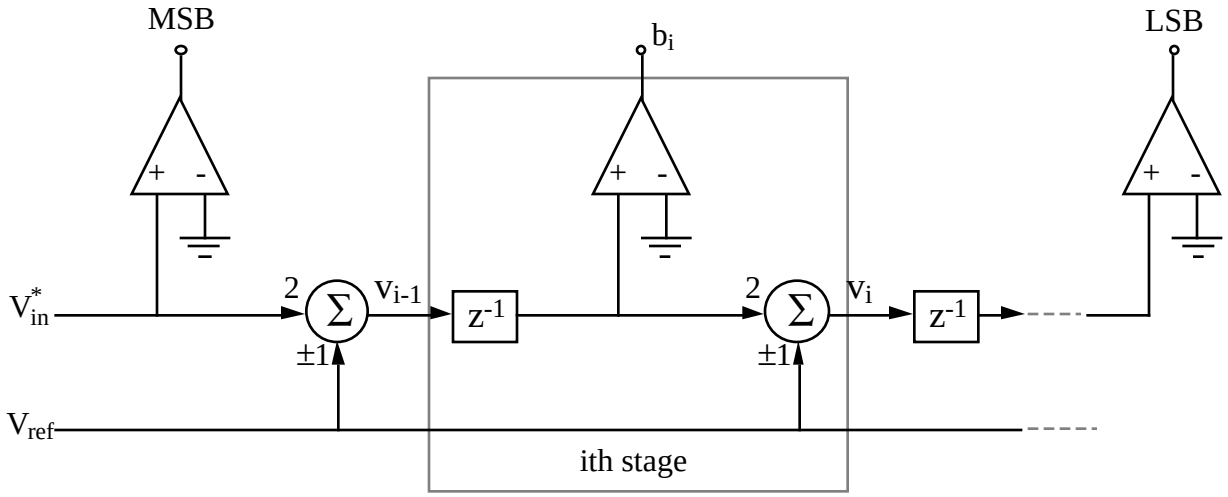


A 1-BIT/PIPE PIPELINE A/D CONVERTER

Single Bit/Stage, N-Stage Pipeline Converter

- Converter in 1 clock cycle using storage registers
- Requires N comparators
- Dependent upon passive component linearity
- Can use error correcting algorithms and self-calibration techniques

Block Diagram of the 1-Bit/Pipe A/D Architecture



$$V_i = 2V_{i-1} - b_i V_{ref} \quad \text{where} \begin{cases} b_i = +1 \text{ if } V_{i-1} > 0 \\ b_i = -1 \text{ if } V_{i-1} < 0 \end{cases}$$

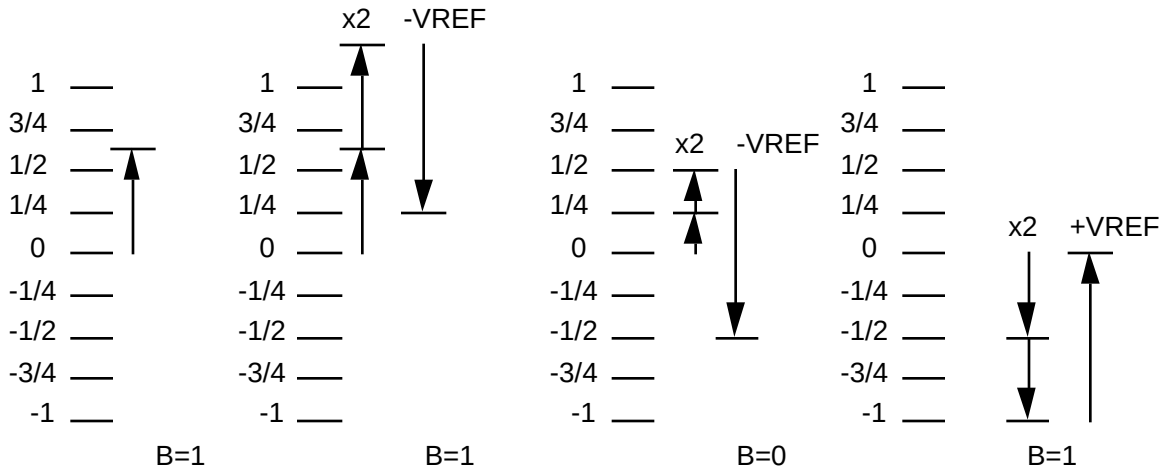
Output of the n-th stage can be written as:

$$V_N = \prod_{i=1}^{N} A_i V_{in} - \left[\sum_{i=1}^{N-1} \left(\prod_{j=i+1}^{N} A_j \right) b_i + b_N \right] V_{ref}$$

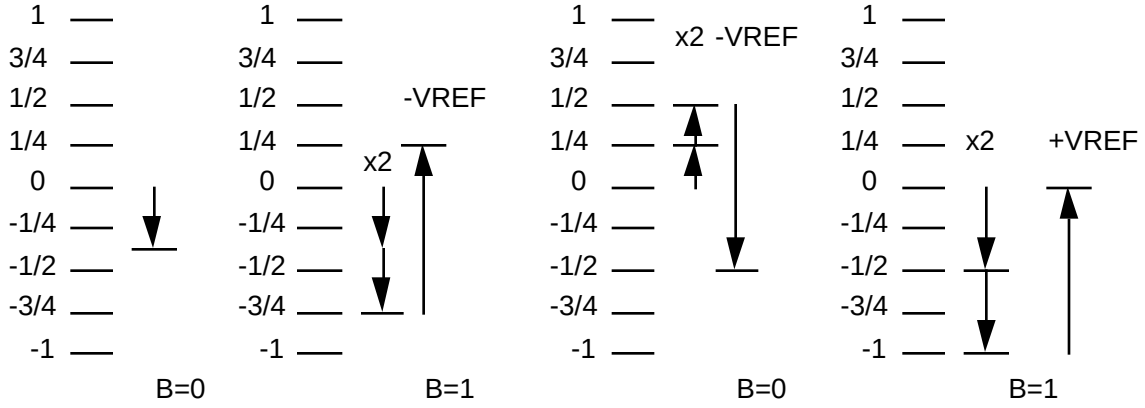
where A_i and b_i are the gain and bit value of the ith stage

Graphical Examples illustrating operation

Example 1

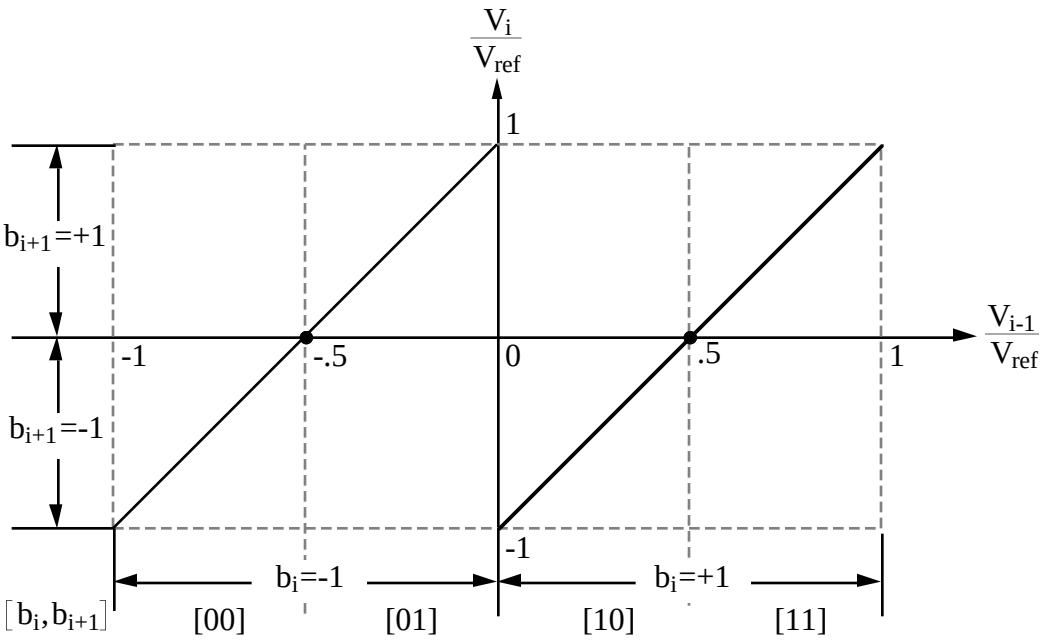


Example 2



IDEAL STAGE PERFORMANCE

ith Stage Plot of: $\frac{V_i}{V_{ref}} = 2\frac{V_{i-1}}{V_{ref}} - b_i$



1.) b_{i+1} must change at 0, and $\pm 0.5V_{ref}$. (when $V_{i-1}=0$ and $\pm 0.5V_{ref}$)

2.) b_i must change at $V_i=0$.

3.) V_i cannot exceed V_{ref}.

4.) V_i should not be less than V_{ref} when $V_{i-1}=\pm V_{ref}$.

IDEAL PERFORMANCE

Example

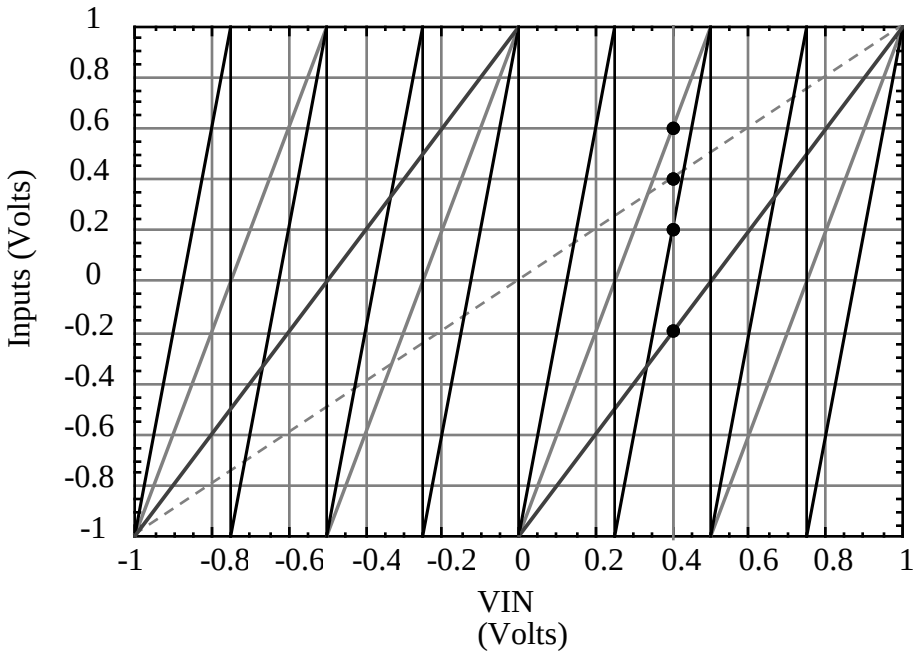
Assume $V_{in}^{*} = 0.4V$ and $V_{ref} = 1V$

Stage i	Input to the ith stage, V_{i-1}	$V_{i-1} > 0$?	Bit i
1	0.4	Yes	1
2	2(0.4000)-1 = -0.200	No	0
3	2(-0.200)+1 = +0.600	Yes	1
4	2(+0.600)-1 = +0.200	Yes	1

Results for various values ov Vin.

Vin	b(i)	v(i+1)	b(i+1)	v(i+2)	b(i+2)	v(i+3)	b(i+3)	v(i+4)	b(i+4)	v(i+5)
-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
-0.9	-1	-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2
-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6
-0.7	-1	-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6
-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2
-0.5	-1	0	1	-1	-1	-1	-1	-1	-1	-1
-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2
-0.3	-1	0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6
-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6
-0.1	-1	0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2
0	1	-1	-1	-1	-1	-1	-1	-1	-1	-1
0.1	1	-0.8	-1	-0.6	-1	-0.2	-1	0.6	1	0.2
0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2	1	-0.6
0.3	1	-0.4	-1	0.2	1	-0.6	-1	-0.2	-1	0.6
0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6	-1	-0.2
0.5	1	0	1	-1	-1	-1	-1	-1	-1	-1
0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6	1	0.2
0.7	1	0.4	1	-0.2	-1	0.6	1	0.2	1	-0.6
0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2	-1	0.6
0.9	1	0.8	1	0.6	1	0.2	1	-0.6	-1	-0.2
1	1	1	1	1	1	1	1	1	1	1

Output Voltage for a 4-stage Converter

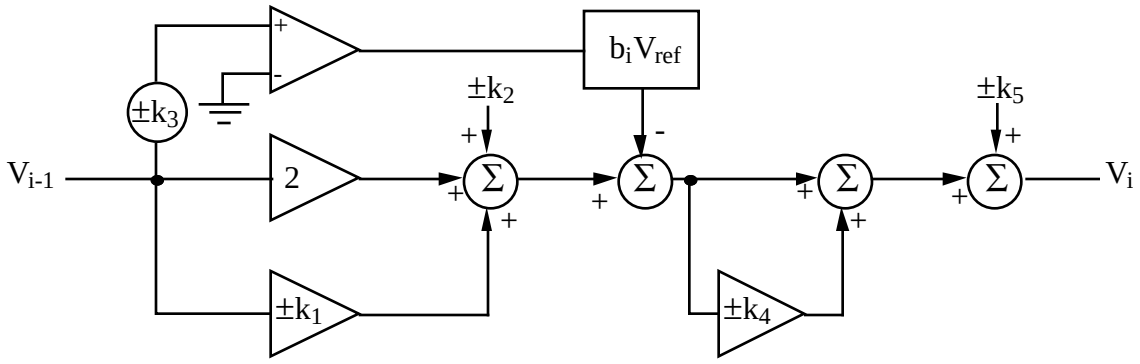


RESOLUTION LIMITS OF THE 1-BIT/STAGE PIPELINE ADC

1st-Order Errors of The 1-Bit/Stage Pipeline ADC

- Gain magnitude and gain matching (k_1)
- Offset of the X2 amplifier and the sample/hold (k_2)
- Comparator offset (k_3)
- Summer magnitude and gain matching (k_4)
- Summer offset (k_5)

Illustration:



$$\boxed{V_i = A_i V_{i-1} + V_{OSi} - b_i A_{si} V_{ref}}$$

where $b_i = \begin{cases} +1 \text{ if } V_{i-1} > \pm k_3 = \pm V_{OCi} \\ -1 \text{ if } V_{i-1} < \pm k_3 = \pm V_{OCi} \end{cases}$

A_i = all gain related errors of the ith stage

V_{OSi} = system offset errors of the ith stage

V_{OCi} = the comparator offset of the ith stage

A_{si} = the gain of the summing junction of the ith stage

Generalization of the First-Order Errors

Extending the ith stage first-order errors to N stages gives:

$$V_N = \prod_{i=1}^{N} A_i V_{in} + \left[\sum_{i=1}^{N-1} \left(\prod_{j=i+1}^{N} A_j \right) V_{OSi} + V_{OSN} \right]$$

$$- V_{ref} \left[\sum_{i=1}^{N-1} \left(\prod_{j=i+1}^{N} A_j \right) A_{si} b_i + A_{sN} b_N \right]$$

Assuming identical errors in each stage gives:

$$V_N = A^N V_{in} + \sum_{i=1}^{N} (A_{N-i}) V_{OS} - V_{ref} \left[\sum_{i=1}^{N} (A^{N-i}) A_s b_i \right]$$

Assuming only the first stage has errors:

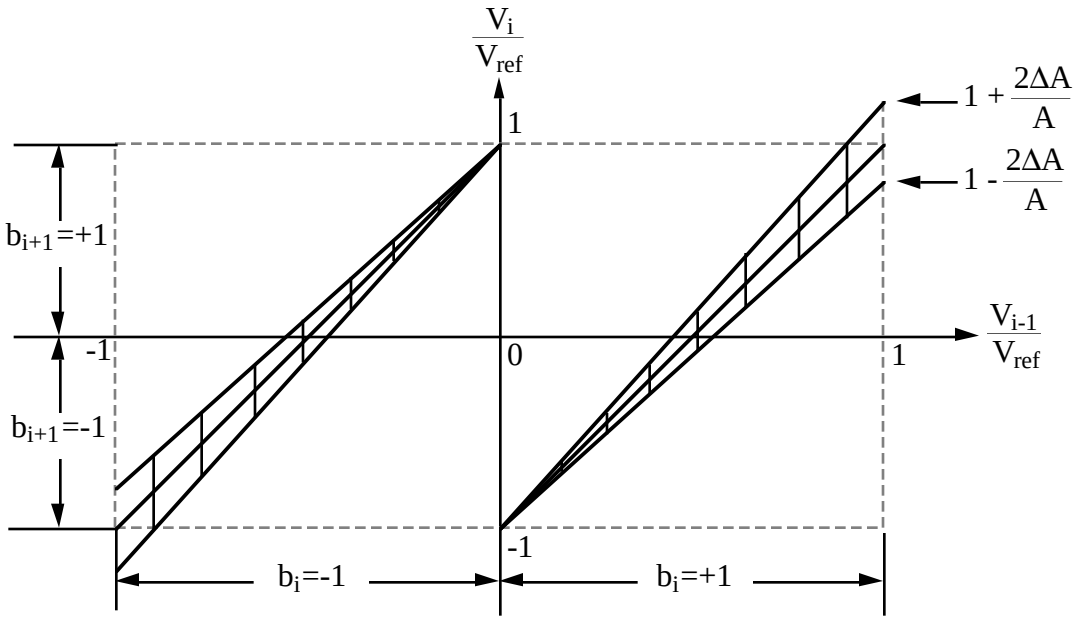
$$V_N = A_1 2^{N-1} V_{in} + 2^{N-1} V_{OS1} - V_{ref} 2^{N-1} A_{s1} b_1 - V_{ref} \sum_{i=2}^{N} (2^{N-i}) b_i$$

Identification of Errors

1. Gain Errors

$$\boxed{2^N(\Delta A/A) < 1} \Rightarrow N=10 \Rightarrow \frac{\Delta A}{A} < \frac{1}{1000}$$

Illustration of gain errors



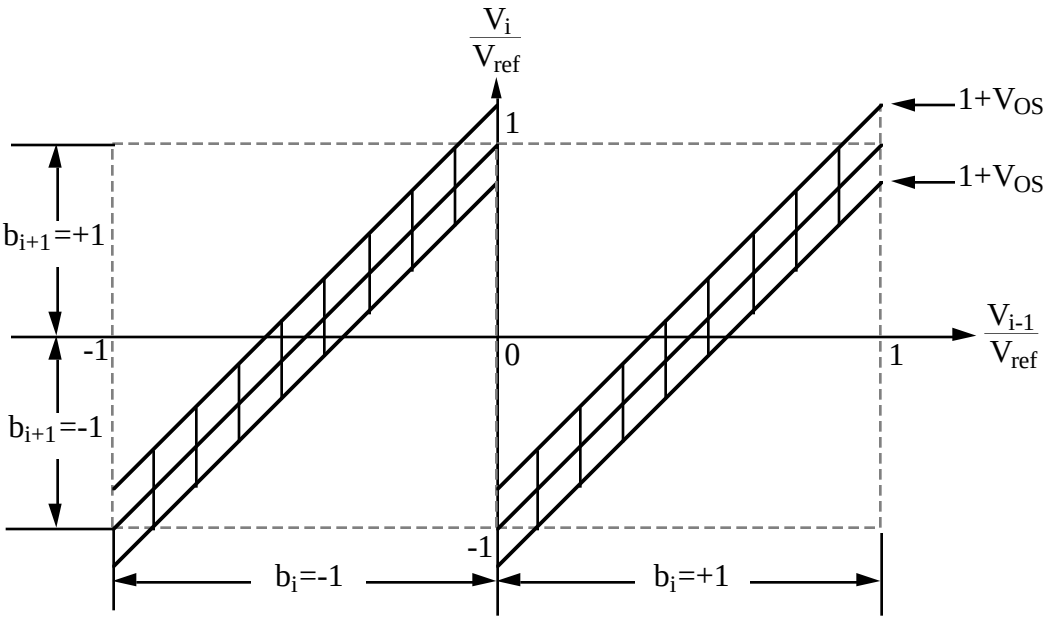
Identification of Errors - Cont'd

2. System Offset Errors

$$V_{OS} < \frac{V_{ref}}{2^N}$$

For N=10 and V_{ref} = 1V, V_{OS} < 1mV

Illustration of system offset error

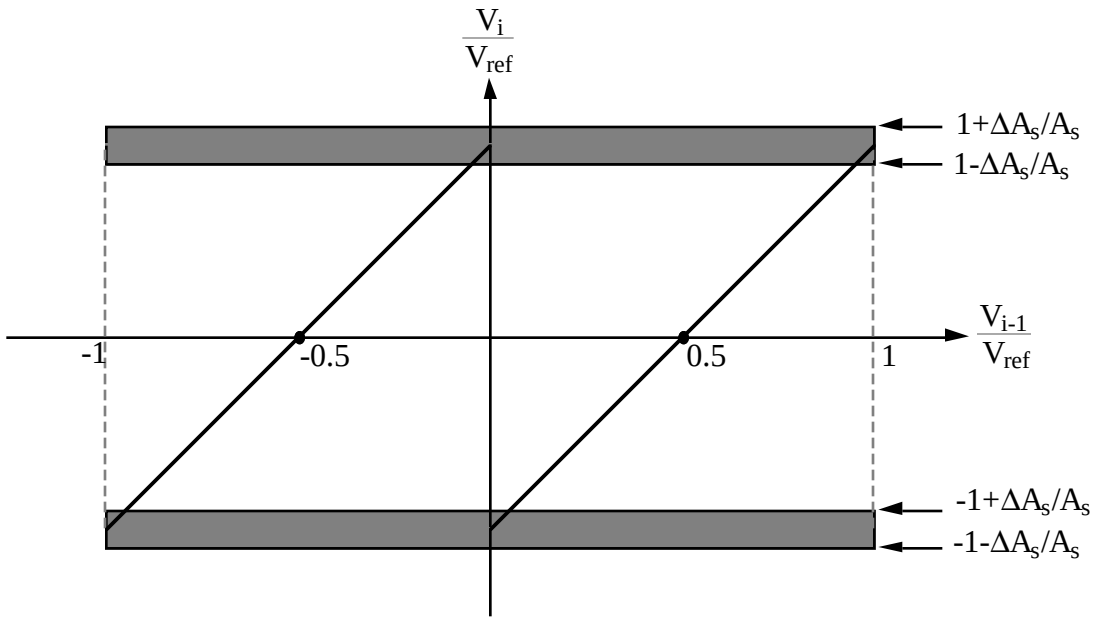


Identification of Errors - Cont'd

3. Summing Gain Error

$$\boxed{\frac{\Delta A_S}{A_S} < \frac{1}{2^N}}$$

For N=10, $\frac{\Delta A}{A} < \frac{1}{1024}$



Identification of Errors - Cont'd

4. Comparator Offset Error

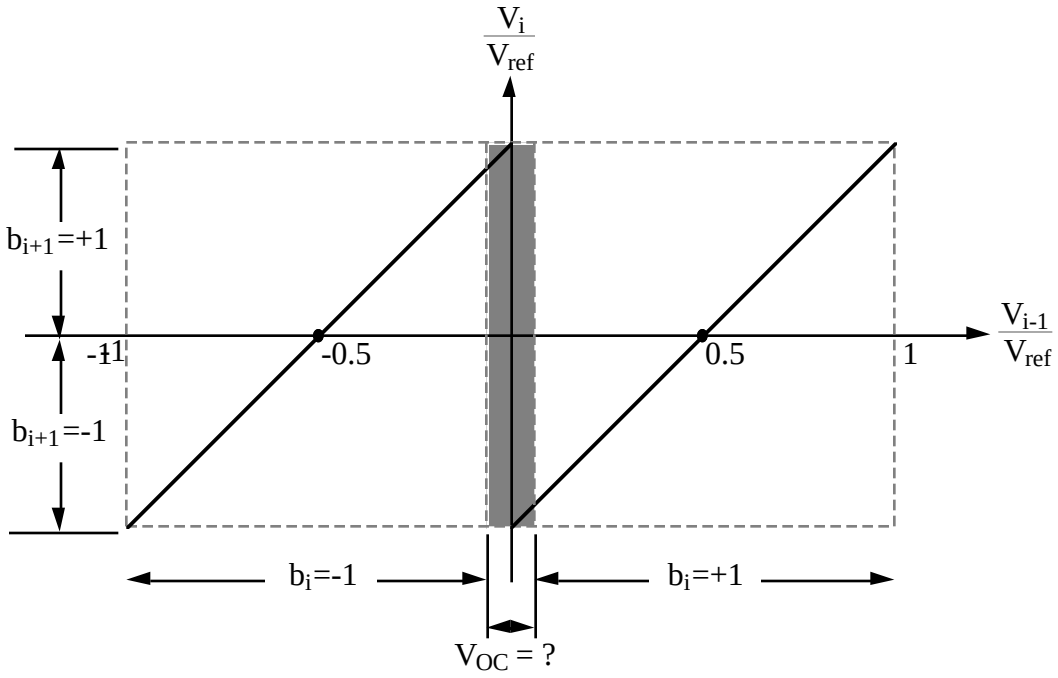
The comparator offset error is any nonzero value of the input to a stage where the stage bit is caused to change. It can be expressed as:

$$V_i = 2V_{i-1} - b_i V_{ref}$$

where

$$b_i = \begin{cases} +1 \text{ if } V_{i-1} > V_{OCi} \\ -1 \text{ if } V_{i-1} < V_{OCi} \end{cases}$$

Illustration of comparator offset error:



SUMMARY

1.) The 1-bit/pipe, pipeline converter which uses standard components including a sample and hold, an amplifier, and a comparator would be capable of realizing at most an 8 or 9 bit converter.

2.) The accuracy of the gains and offset of the first stage of an N-Bit converter must be within 0.5LSB.

3.) The accuracy of the gains and offset of a stage diminishes with the remaining number of stages to the output of the converter.

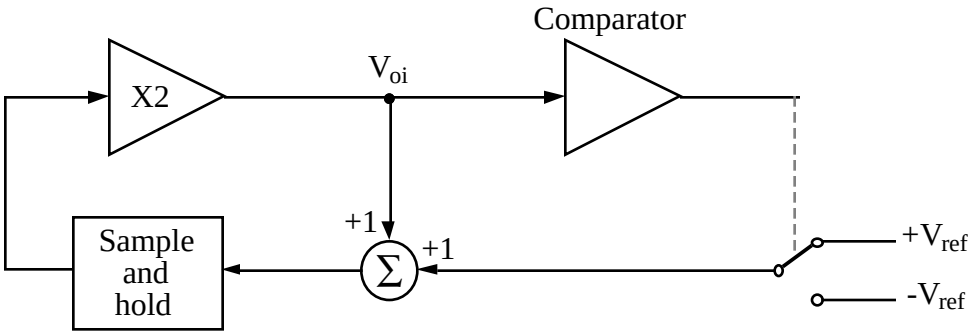
4.) Error correction and self-calibrating techniques are necessary in order to realize the potential resolution capability of the 1-bit/'stage pipeline ADC.

Cyclic Algorithmic A/D Converter

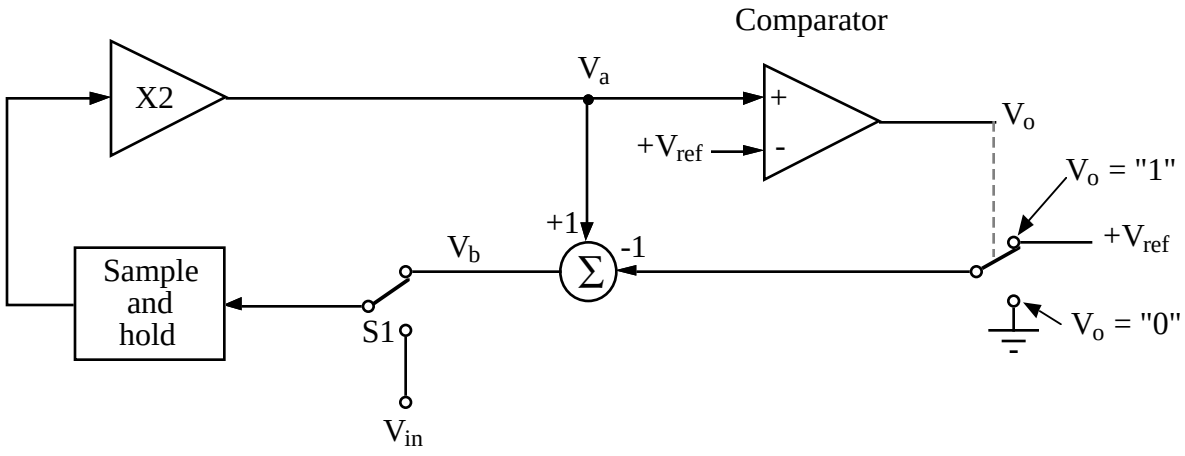
The output of the ith stage of a pipeline A/D converter is

$$V_{oi} = (2V_{o,i-1} - b_i V_{REF})z^{-1}$$

If V_{oi} is stored and feedback to the input, the same stage can be used for the conversion. The configuration is as follows:



Practical implementation:



Algorithmic ADC - Example

Assume that $V_{in}^* = 0.8V_{REF}$. The conversion proceeds as;

1.) $0.8V_{REF}$ is sampled and applied to the X2 amplifier by S1.

2.) $V_a(0)$ is $1.6V_{REF}$ (b_1=1) which causes $-V_{REF}$ to be subtracted from $V_a(0)$ giving

$V_b(0) = 0.6V_{REF}$

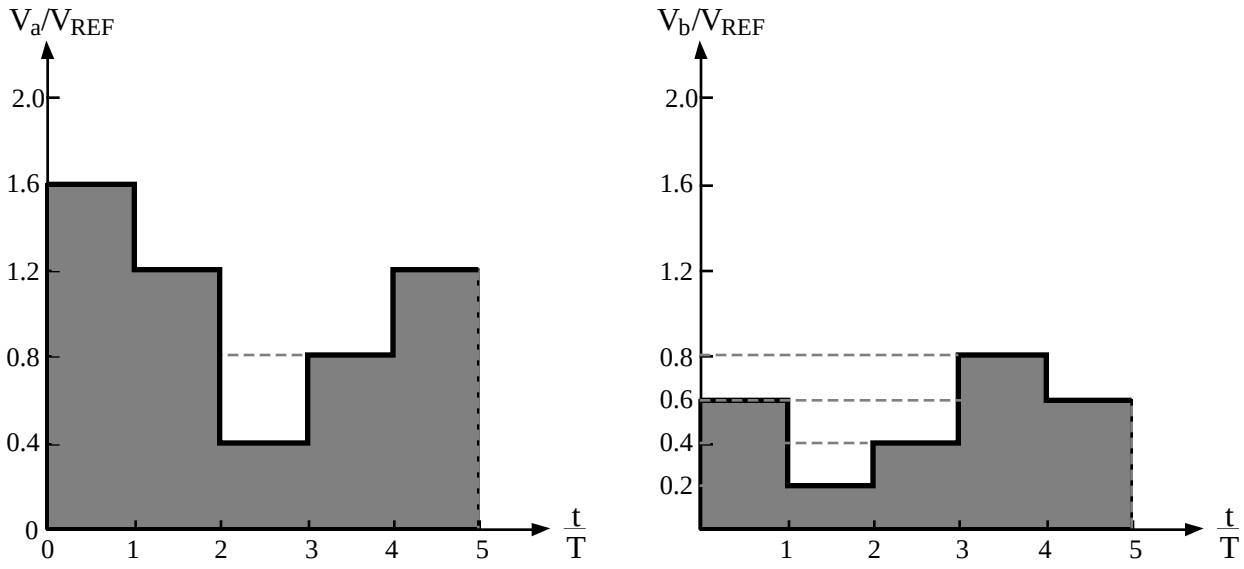
3.) In the next cycle, $V_a(1)$ is $1.2V_{REF}$ (b_2=1) and $V_b(1)$ is $0.2V_{REF}$.

4.) The next cycle gives $V_a(2) = 0.4V_{REF}$ (b_3=0) and $V_b(2)$ is $0.4V_{REF}$.

5.) The next cycle gives $V_a(3) = 0.8V_{REF}$ (b_4=0) and $V_b(3)$ is $0.8V_{REF}$.

6.) Finally, $V_a(4) = 1.6V_{REF}$ (b_5=1) and $V_b(4) = 0.6V_{REF}$.

$\therefore$ The digital word is 11001. $\Rightarrow$ $V_{analog} = 0.78125V_{REF}$.



Algorithmic A/D Converters-Practical Results

- Only one accurate gain-of-two amplifier required.
- Small area requirements
- Slow conversion time - nT.
- Errors: Finite op amp gain, input offset voltage, charge injection, capacitance voltage dependence.

Practical Converter

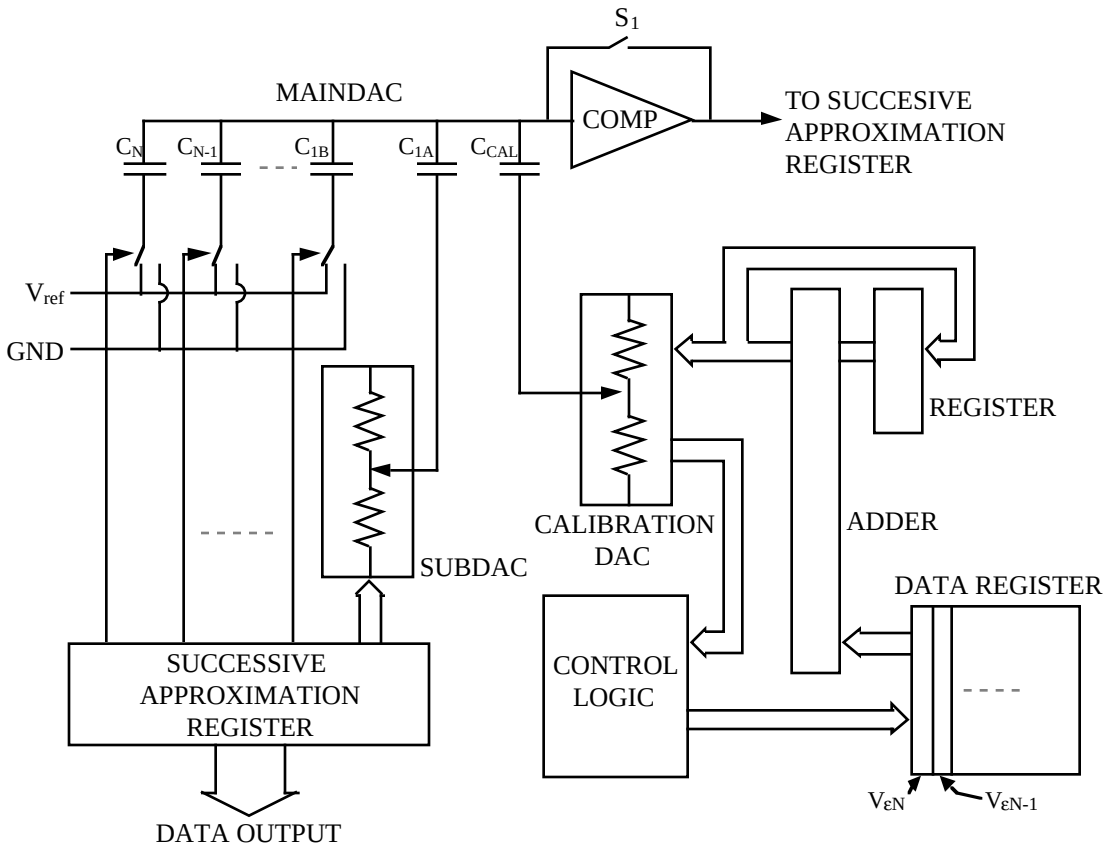
12 Bits

Differential linearity of 0.019% (0.8LSB)

Integral linearity of 0.034% (1.5LSB)

Sample rate of 4KHz.

SELF-CALIBRATING ADC's



Main ADC is an N-bit charge scaling array.

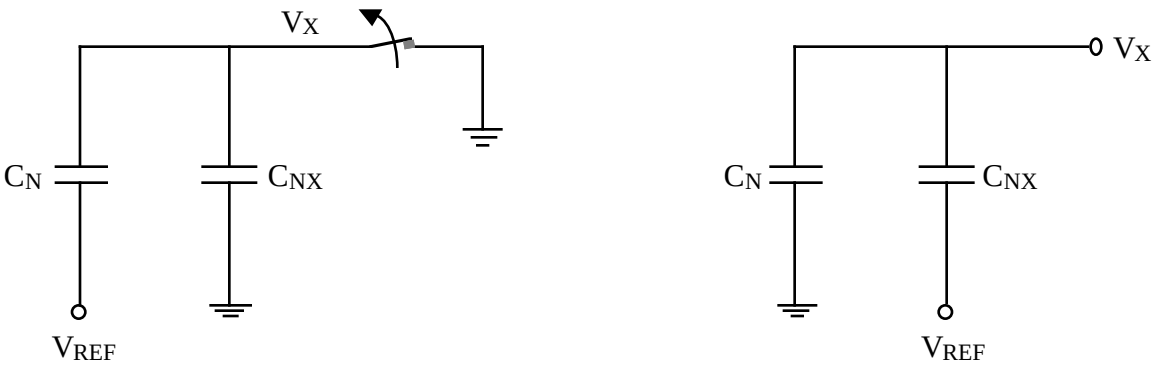
Sub DAC is an M-bit voltage scaling array.

Calibration DAC is an M+2 bit voltage scaling array.

This is an voltage-scaling, charge-scaling A/D converter with (N+M)- bits resolution.

Self-Calibration Procedure

During calibration cycles, the nonlinearity factors caused by capacitor mismatching are calibrated and stored in the data register for use in the following normal conversion cycles. The calibration procedure begins from MSB by connecting C_N to V_{REF} and the remaining capacitors C_{NX} to GND, then exchange the voltage connection as follows:



where $C_{NX} = C_{1B} + C_{1A} + ... + C_{N-1}$

The final voltage V_X after exchanging the voltage connections is

$$V_X = V_{REF} \frac{C_{NX} - C_N}{C_{NX} + C_N}$$

If the capacitor ratio is accurate and $C_{NX} = C_N \Rightarrow V_X = 0$,

otherwise $V_X \neq 0$. This residual voltage V_X is digitized by the calibration DAC. Other less significant bits are calibrated in the same manner.

After all bits are calibrated, the normal successive-approximation conversion cycles occurs. The calibrated data stored in the data register is converted to an analog signal by calibration DAC and is fed to the main DAC by C_{CAL} to compensate the capacitor mismatching error.

Self-Calibrating ADC Performance

Supply voltage ± 5V

Resolution of 16 bits

Linearity of 16 bits

Offset less than 0.25 LSB

Conversion time for 0.5 LSB linearity:

12 μs for 12 Bits

80 μs for 16 Bits.

RMS noise of 40 μV.

Power dissipation of 20 mW (excludes logic)

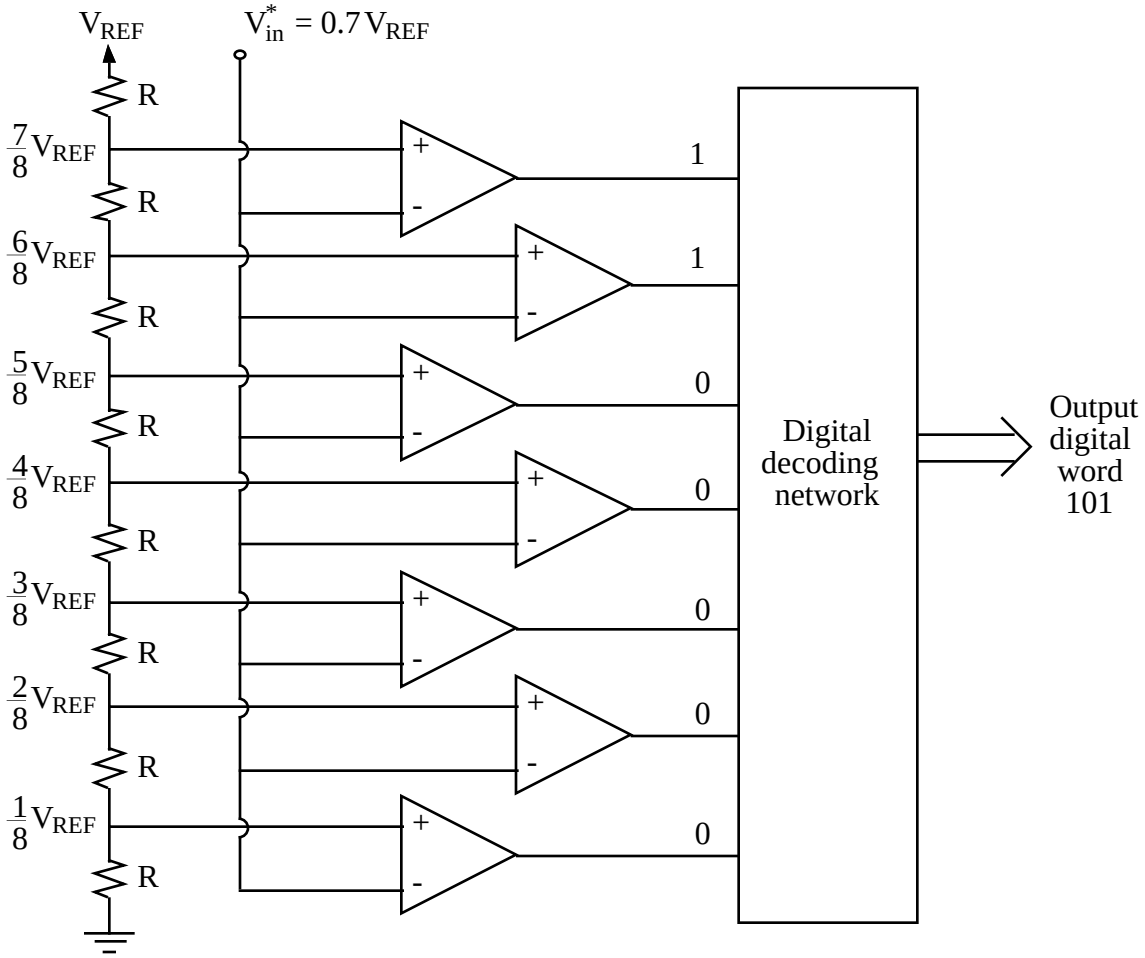
Area of 7.5 mm (excludes logic).

X.9 - HIGH_SPEED_ADC's

Conversion Time ≈ T (T = clock period)

- Flash or parallel
- Time interleaving
- Pipeline - Multiple Bits
- Pipeline - Single Bit

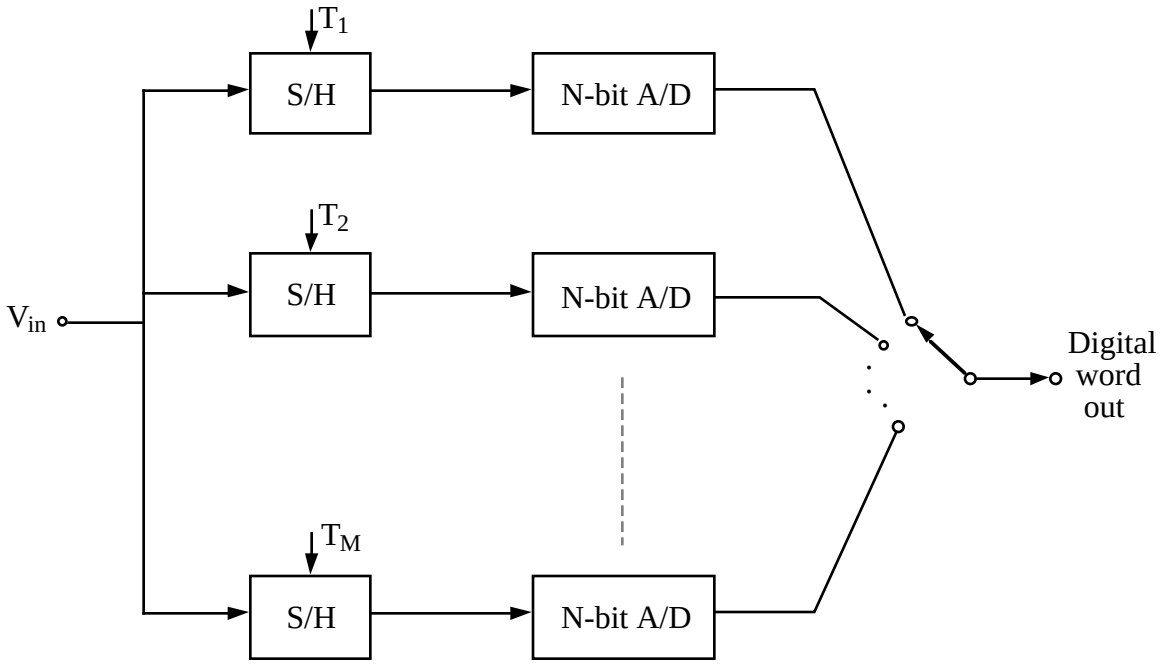
FLASH A/D CONVERTER

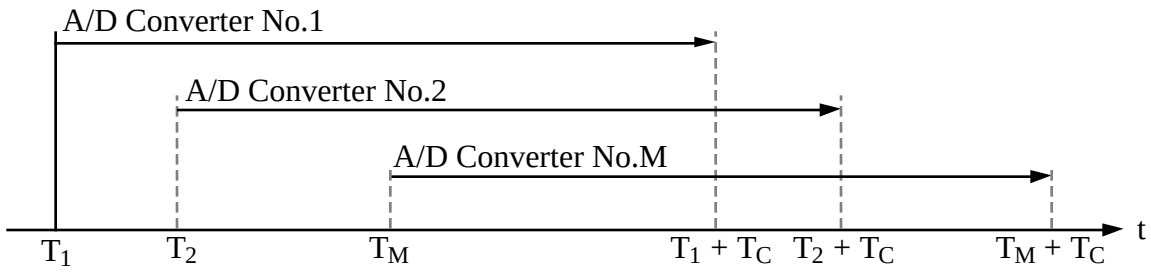


- Fast conversion time, one clock cycle
- Requires 2^N-1 comparators
- Maximum practical bits is 6 or less
- 6 bits at 10 MHz is practical

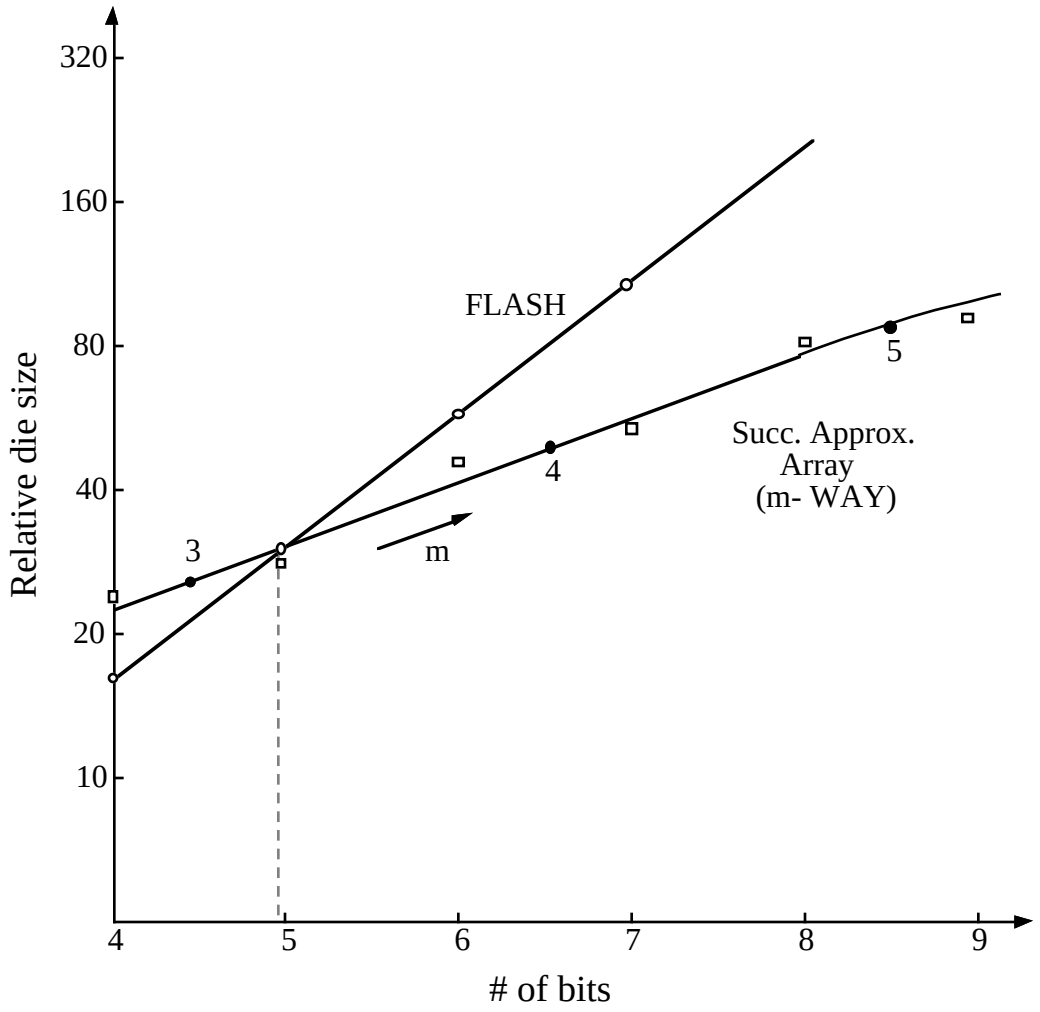
Time-Interleaved A/D Converter Array

Use medium speed, high bit converters in parallel.



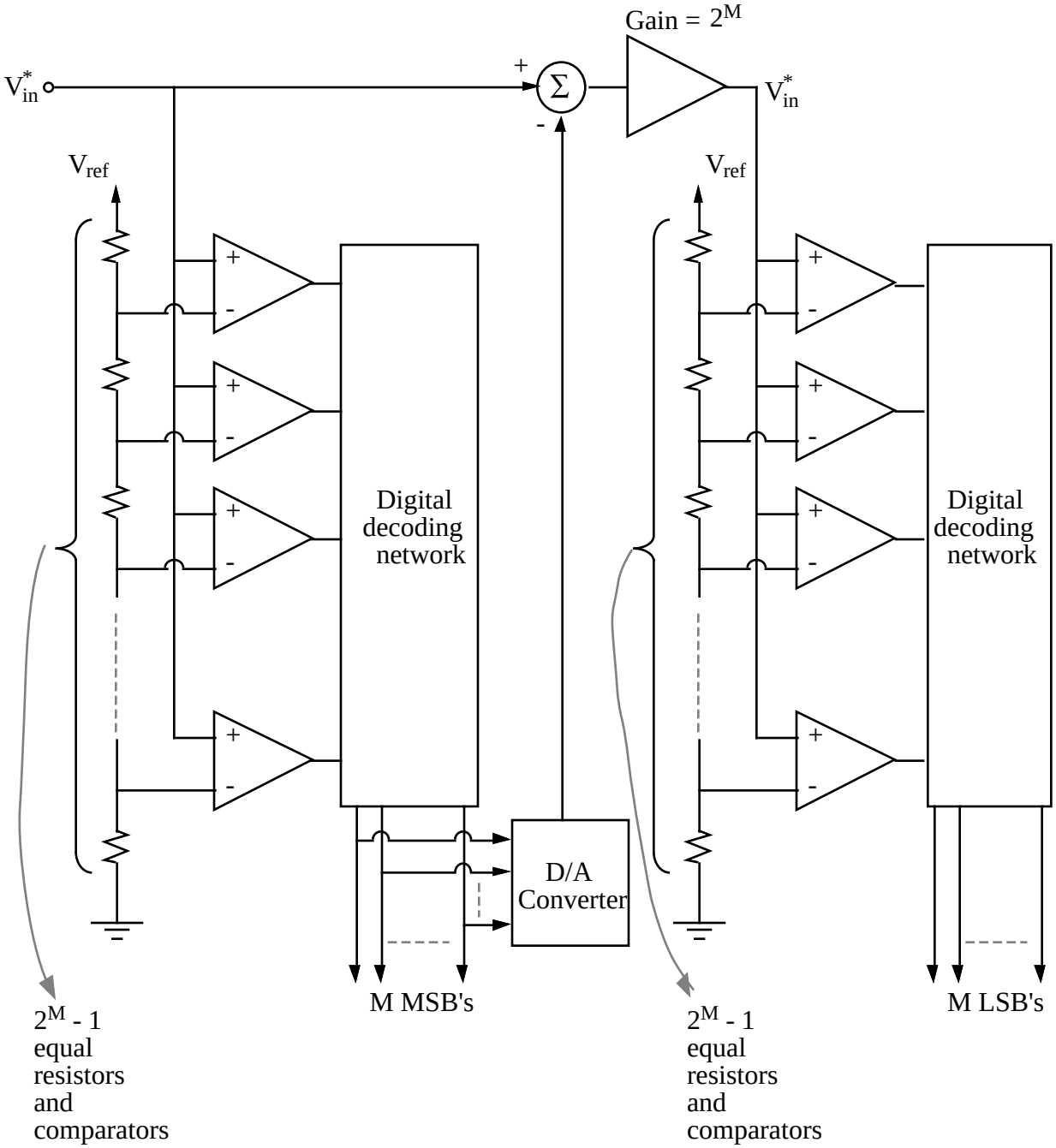


Relative Die Size vs. Number of Bits



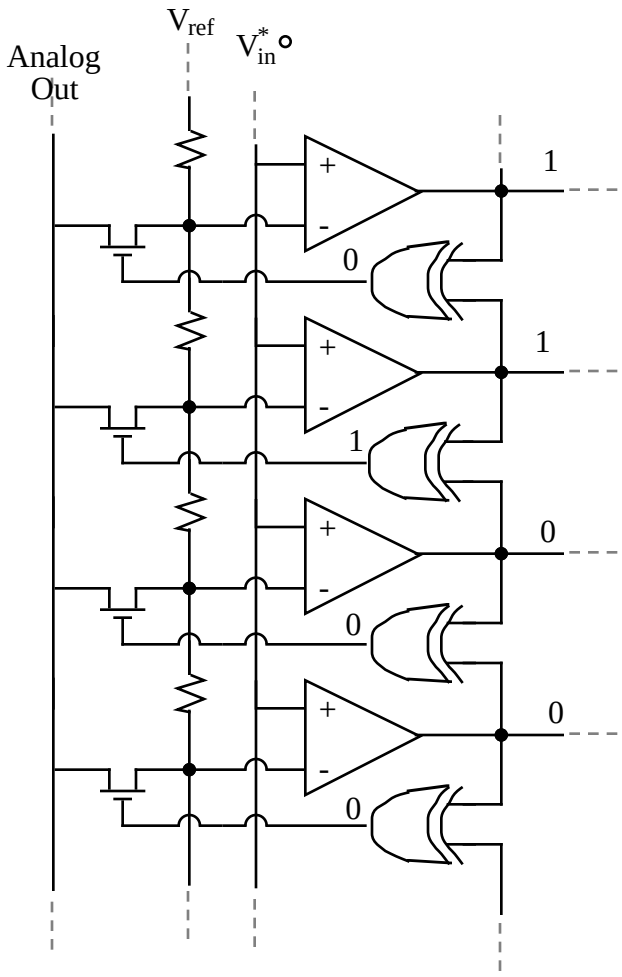
2M-BIT, PARALLEL-CASCADE ADC

- Compromise between speed and area
- 8-bit, 1M Hz.



Conversion of Digital back to Analog for Pipeline Architectures

Use XOR gates to connect to the appropriate point in the resistor divider resulting in the analog output corresponding to the digital output.

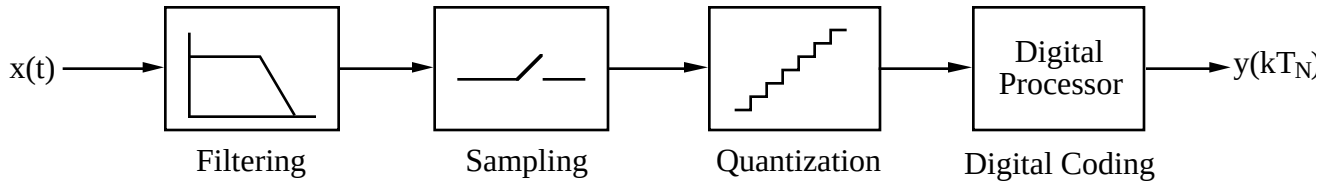


X.10 - OVERSAMPED (Δ-∑) A/D CONVERTER

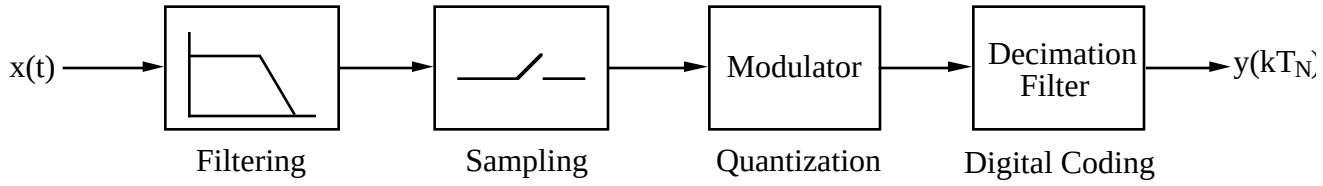
NYQUIST VERSUS OVERSAMPLED A/D CONVERTERS

Oversampling A/D converters use a sampling clock frequency(f_S) much higher than the Nyquist rate(fN).

Conventional Nyquist ADC Block Diagram:



Oversampling ADC Block Diagram



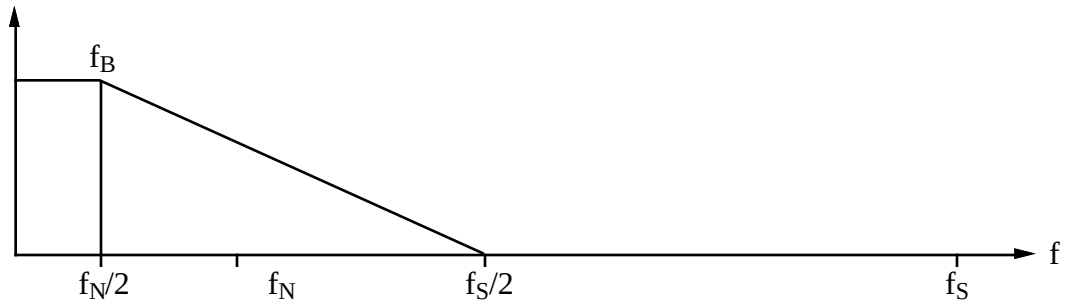
The anti-aliasing filter at the input stage limits the bandwidth of the input signal and prevents the possible aliasing of the following sampling step. The modulator pushes the quantization noise to the higher frequency and leaves only a small fraction of noise energy in the signal band. A digital low pass filter cuts off the high frequency quantization noise. Therefore, the signal to noise ratio is increased.

ANTI-ALIASING FILTER

The anti-aliasing filter of an oversampling ADC requires less effort than that of a conventional ADC. The frequency response of the anti-aliasing filter for the conventional ADC is sharper than the oversampling ADC.

Conventional ADC's Anti-Aliasing Filter

Oversampling ADC's Anti-Aliasing Filter



f_B : Signal Bandwidth

f_N : Nyquist Frequency, $f_N = 2f_B$

f_S : Sampling Frequency and usually $f_S >> f_N$

M : Oversampling ratio, $M = \frac{f_S}{f_N}$

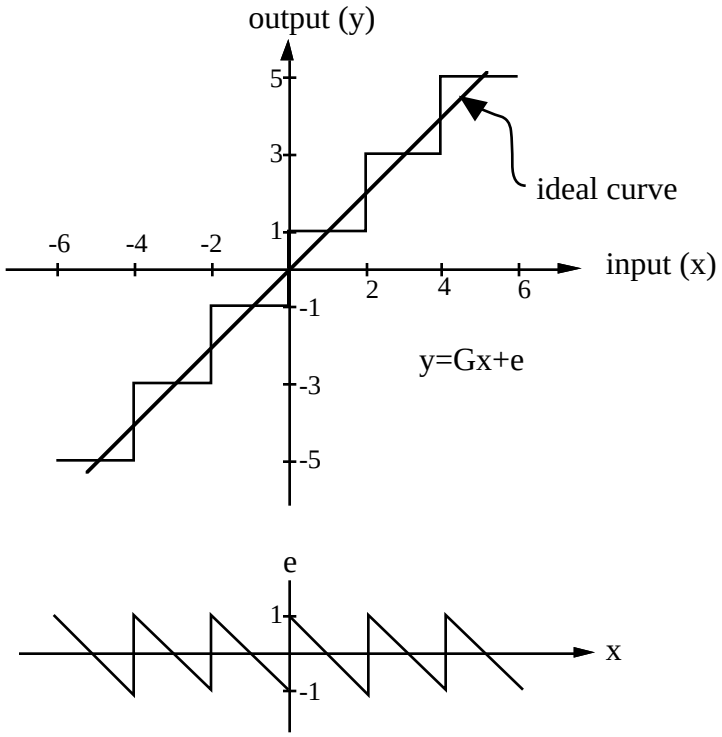
So the analog anti-aliasing filter of an oversampling ADC is less expensive than the conventional ADC. If M is sufficiently large, the analog anti-aliasing filter is simply an RC filter.

QUANTIZATION

Conventional ADC's Quantization

The resolution of conventional ADCs is determined by the relative accuracy of their analog components. For a higher resolution, self-calibration technique can be adopted to enhance the matching accuracy.

Multilevel Quantizer:



The quantized signal y can be represented by

$$y = Gx + e$$

where,

G = gain of ADC, normally = 1
e = quantization error

Conventional ADC's Quantization - Cont'd

The mean square value of quantization error, e, is

$$e^2_{rms} = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e(x)^2\,dx = \frac{\Delta^2}{12}$$

where

$$\Delta = \text{the quantization level of an ADC (typically} \frac{VREF}{2^N})$$

When a quantized signal is sampled at f_S (= $1/\tau$), all of its noise power folds into the frequency band from 0 to $f_S/2$. If the noise power is white, then the spectral density of the sampled noise is

$$E(f) = e_{rms}\left(\frac{2}{f_S}\right)^{1/2} = e_{rms}\sqrt{2\tau}$$

where

$$\tau = 1/f_S \quad \text{and} \quad f_S = \text{sampling frequency}$$

The inband noise energy n_o is

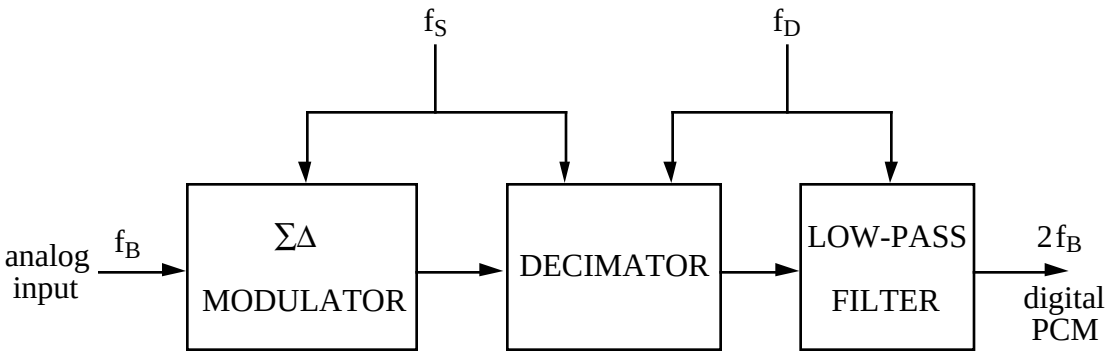
$$n_o^2 = \int_0^{f_B} E^2(f)df = e^2_{rms}\,(2f_B\tau) = e^2_{rms}\left(\frac{2f_B}{f_S}\right) = \frac{e^2_{rms}}{M}$$

$$n_o = \frac{e_{rms}}{\sqrt{M}}$$

The oversampling ratio $M = \frac{f_S}{2f_B}$

Therefore, each doubling of the sampling frequency decreases the in-band noise energy by 3 dB, and increases the resolution by 0.5 bit. This is not a very efficient method of reducing the inband noise.

OVERSAMPLING ADC



Oversampling ADCs consist of a ∑Δ modulator, a decimator (down-sampler), and a digital low pass filter.

∑Δ modulator

Also called the noise shaper because it can shape the quantization noise and push majority of the noise to high frequency band. It modulates the analog input signal to a simple digital code, normally is one bit, using a sampling rate much higher the Nyquist rate.

Decimator

Also called the down-sampler because it down samples the high frequency modulator output into a low frequency output.

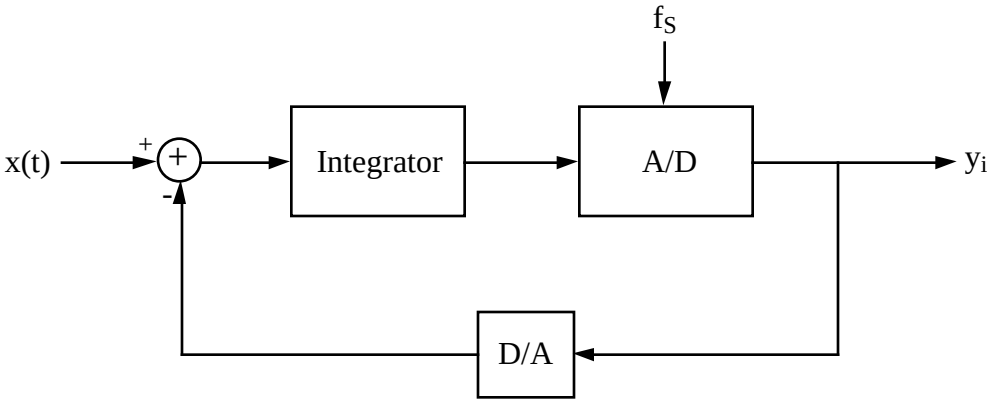
Low-pass filter

Use digital low pass filter to cut off the high frequency quantization noise and preserve the input signal.

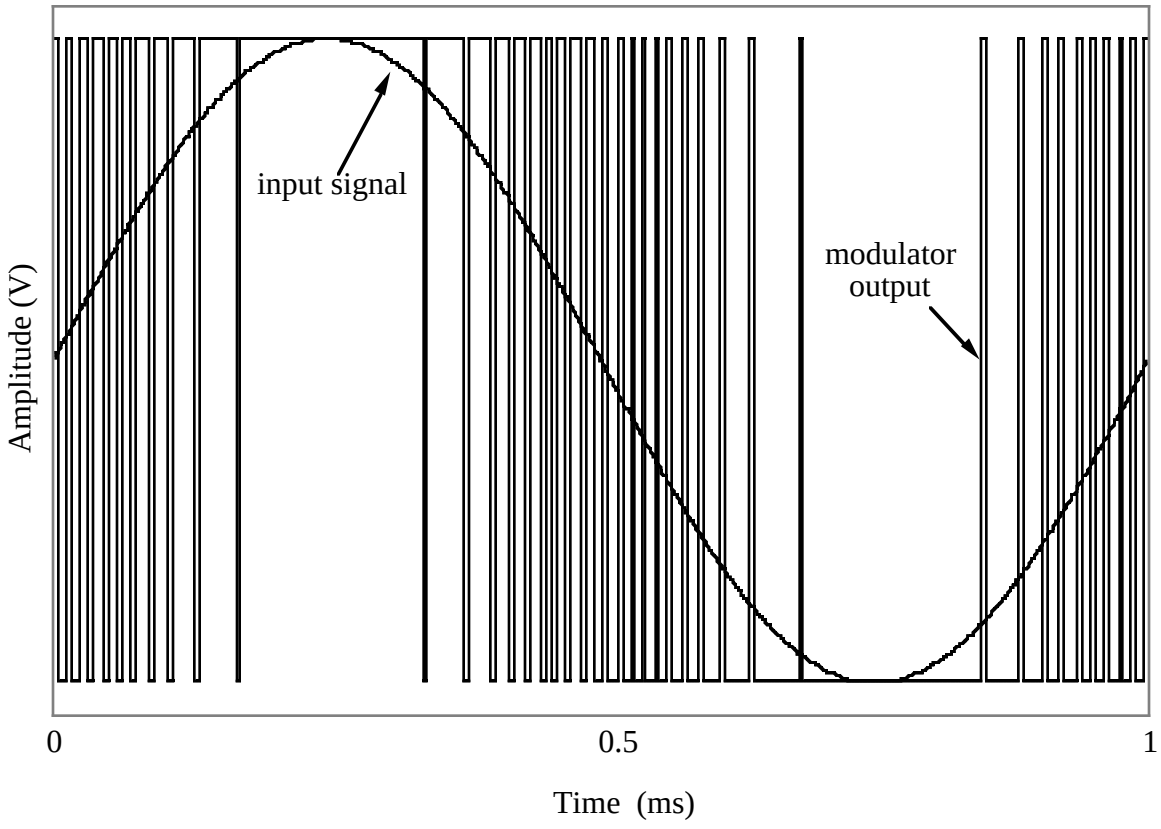
Sigma-Delta (∑Δ) Modulator

First Order ∑Δ Modulator

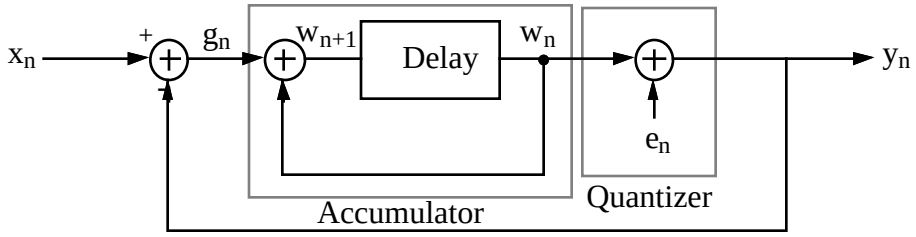
The open loop quantizer in a conventional ADC can be modified by adding a closed loop to become a ∑Δ modulator.



Modulator Output



First-Order ∑Δ Modulator



$$y_n = w_n + e_n$$

(1)

$$w_{n+1} = g_n + w_n = x_n - y_n + w_n$$

$$= x_n -(w_n + e_n) + w_n = x_n - e_n$$

(2)

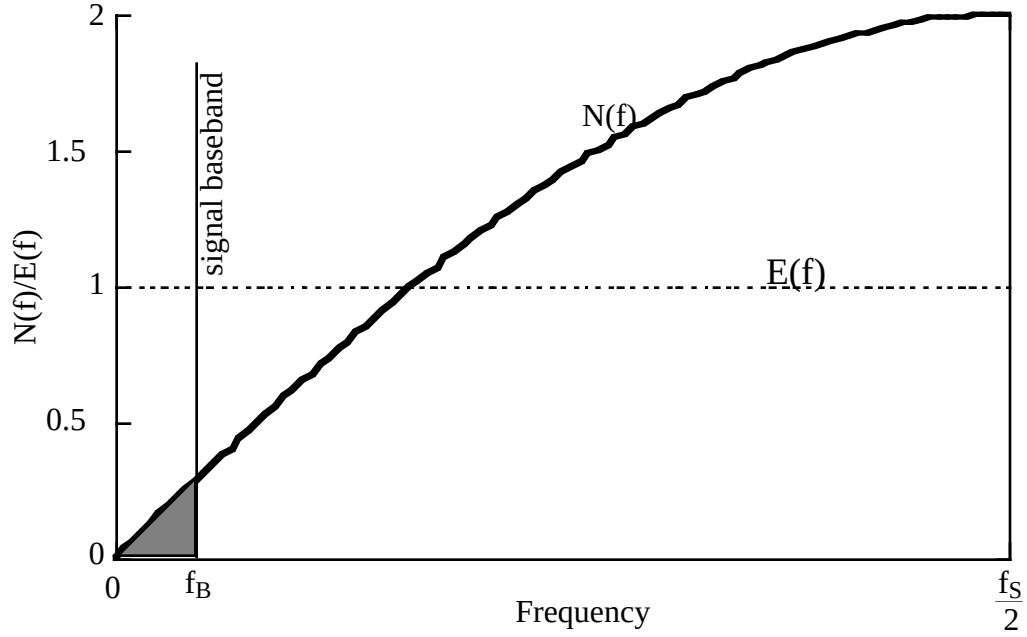
Therefore, $w_n = x_{n-1} - e_{n-1}$, which when substituted into (1) gives

$$y_n = x_{n-1} + (e_n - e_{n-1})$$

The output of ∑Δ modulator y_n is the input signal delayed by one clock cycle x_{n-1}, plus the quantization noise difference $e_n - e_{n-1}$. The modulation noise spectrum density of $e_n - e_{n-1}$ is

$$N(f) = E(f)\left|1 - z^{-1}\right| = E(f)\left|1 - e^{-j\omega\tau}\right| = 2E(f)\sin\left(\frac{\omega\tau}{2}\right) = 2e_{rms}\sqrt{2\tau}\ \sin\left(\frac{\omega\tau}{2}\right)$$

Plot of Noise Spectrum



First Order ∑Δ Modulator-Cont'd

The noise power in the signal band is

$$n_o^2 = \int_0^{f_B} |N(f)|^2 df = \int_0^{f_B} \left(2e_{rms}\sqrt{2\tau}\sin\left(\frac{\omega\tau}{2}\right)\right)^2 df$$

$$n_o^2 = \int_0^{f_B} \left(2e_{rms}\sqrt{2\tau}\,(\pi f\tau)\right)^2 df$$

$$\text{where } \sin\left(\frac{\omega\tau}{2}\right) = \sin\left(\frac{2\pi f}{2f_S}\right) = \sin\left(\frac{\pi f}{f_S}\right) \approx \pi f\tau$$

$$\text{if } f_S >> f$$

Therefore,

$$n_o^2 \approx (2\tau)^3\pi^2\, e_{rms}^2 \int_0^{f_B} f^2\, df = \frac{e_{rms}^2\pi^2(2\tau f_B)^3}{3}$$

$$\text{where, } \quad f_S >> f_B$$

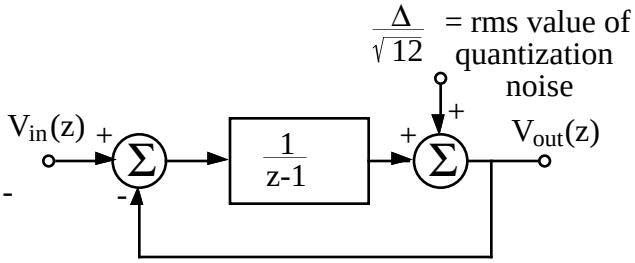
Thus,

$$n_o = e_{rms}\frac{\pi}{\sqrt{3}}\left(2f_B\tau\right)^{3/2} = e_{rms}\frac{\pi}{\sqrt{3}}M^{-3/2}$$

Each doubling of the oversampling ratio reduces the modulation noise by 9 dB and increase the resolution by 1.5 bits.

Oversampling Ratio Required for a First-Order ΔΣ Modulator

A block diagram for a first-order, sigma-delta modulator is shown in the z-domain. Find the magnitude of the output spectral noise with $V_{IN}(z) = 0$ and determine the bandwidth of a 10-bit analog-to-digital converter if the sampling frequency, f_S, is 10 MHz.



Solution

$$V_{out}(z) = e_{rms} + \left(\frac{1}{z-1}\right)[V_{in}(z) - V_{out}(z)]$$

or

$$V_{out}(z) = \left(\frac{z-1}{z}\right) e_{rms} \text{ if } V_{in}(z) = 0 \rightarrow V_{out}(z) = (1-z^{-1})e_{rms}$$

$$|N(f)| = E(f)\left|1 - e^{-j\omega\tau}\right| = 2E(f)\sin\left(\frac{\omega\tau}{2}\right) = 2\sqrt{\frac{2}{f_S}}\, e_{rms}\sin\left(\frac{\omega\tau}{2}\right)$$

The noise power is found as

$$n_o^2(f) = \int_0^{f_B} |N(f)|^2\, df = \int_0^{f_B}\left(2\sqrt{\frac{2}{f_S}}e_{rms}\right)^2 \sin^2\left(\frac{2\pi f\tau}{2}\right) df$$

Let $\sin\left(\frac{2\pi f\tau}{2}\right) \approx \pi f\tau$ if $f_S >> f_B$. Therefore,

$$n_o^2(f) = 4\left(\frac{2}{f_S}\right)e_{rms}^2(\pi\tau)^2\int_0^{f_B} f^2\, df = \frac{8\pi^2}{3}e_{rms}^2\left(\frac{f_B}{f_S}\right)^3$$

or

$$n_o(f) = \sqrt{\frac{8}{3}}\,\pi\cdot e_{rms}\left(\frac{f_B}{f_S}\right)^{3/2} \le \frac{VREF}{2^{10}}$$

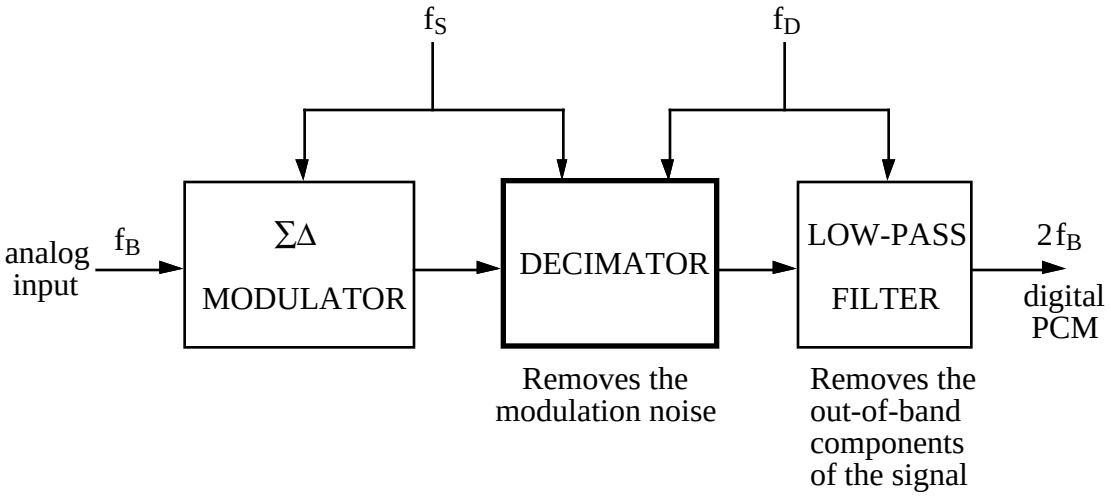
Solving for f_B/f_S gives (using Δ in e_{rms} term is equal to VREF)

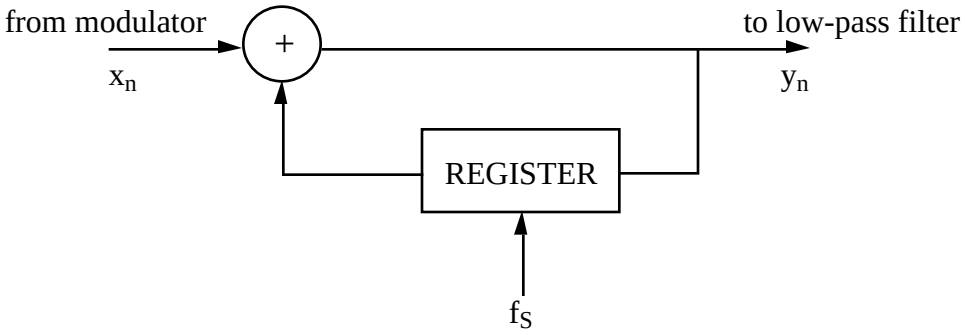
$$\frac{f_B}{f_S} = \left[\left(\frac{\sqrt{12}\sqrt{3}}{\sqrt{8}\,\pi}\right)\frac{1}{2^{10}}\right]^{2/3} = [0.659\text{x}10^{-3}]^{2/3} = 0.007576$$

$$f_B = 0.007576\cdot 10\text{MHz} = 75.76\text{kHz}.$$

Decimator (down-sampling)

The one-bit output from the ΣΔ modulator is at very high frequency, so we need a decimator (or down sampler) to reduce the frequency before going to the digital filter.





$$y_n = \frac{1}{N}\sum_{N=0}^{N} x_n \quad \text{, where } N = \frac{f_S}{f_D} \text{ = down-sampling ratio}$$

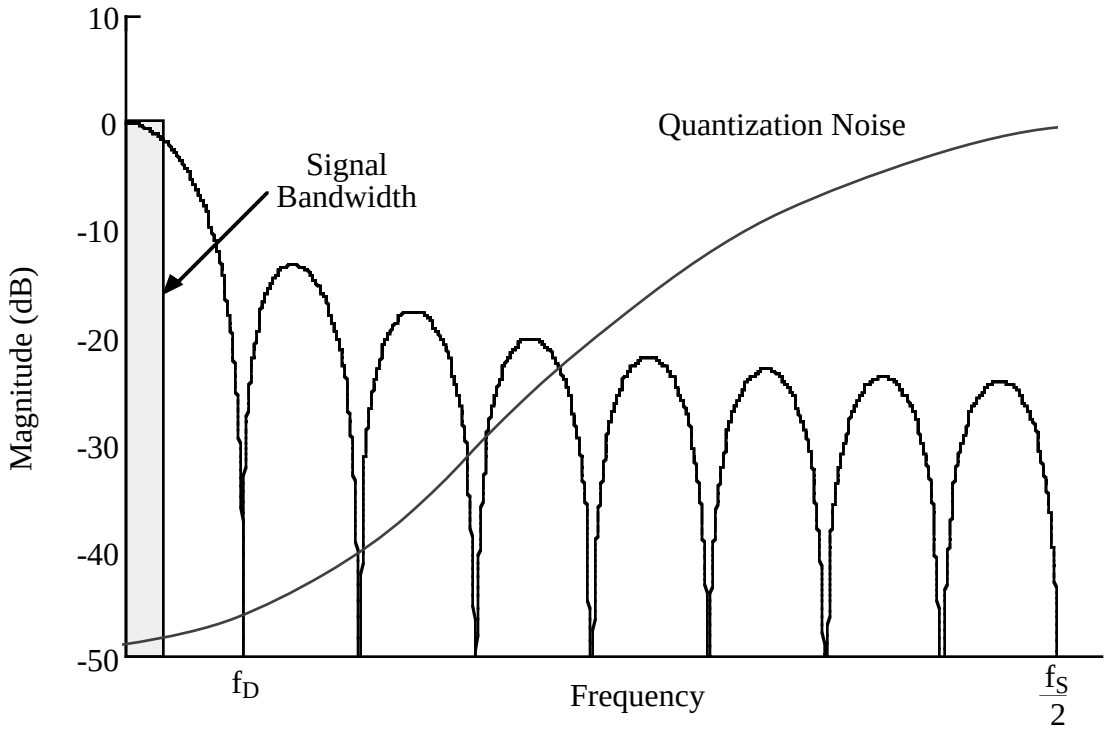
The transfer function of decimator is

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1}{N}\sum_{i=0}^{N-1} z^{-i} = \frac{1}{N}\frac{1 - z^{-N}}{1 - z^{-1}}$$

$$H(e^{j\omega\tau}) = \frac{\text{sinc}(\pi f N\tau)}{\text{sinc}(\pi f\tau)}$$

Frequency Spectrum of the Decimator

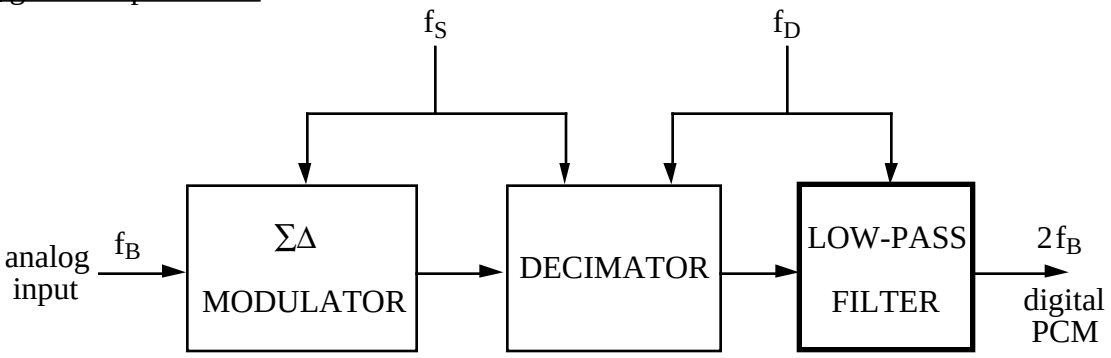
$$H(e^{j\omega\tau}) = \frac{\text{sinc}(\pi f N\tau)}{\text{sinc}(\pi f\tau)}$$



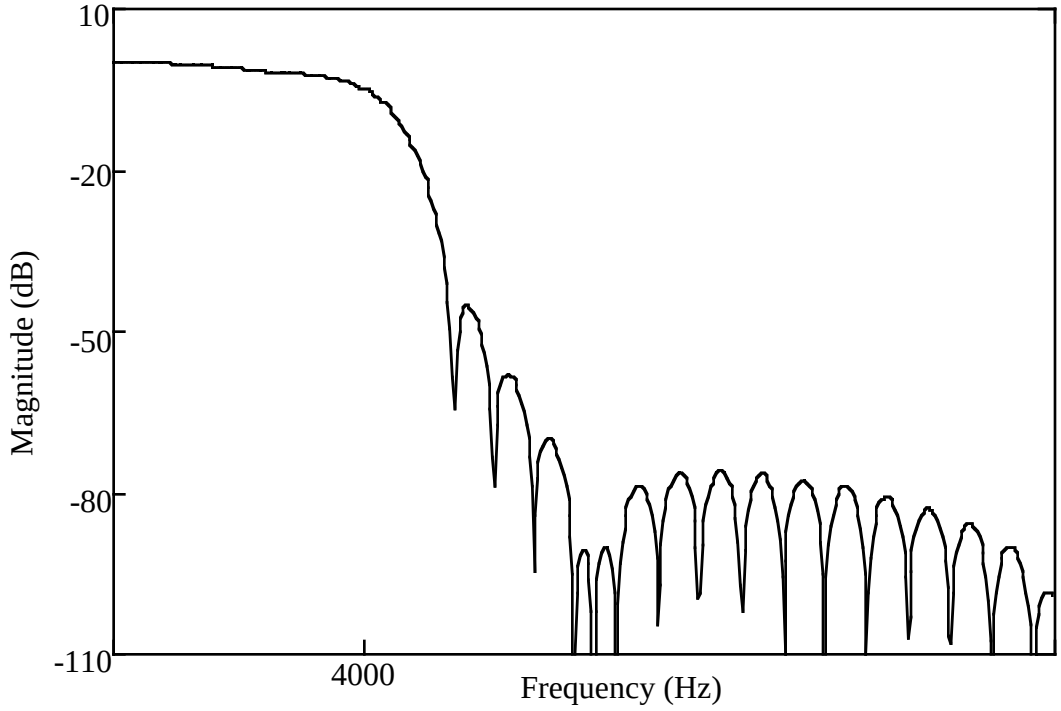
f_D = intermediate decimation frequency

When the modulation noise is sampled at f_D, its components in the vicinity of f_D and the harmonics of f_D fold into the signal band. Therefore, the zeros of the decimation filter must be placed at these frequencies.

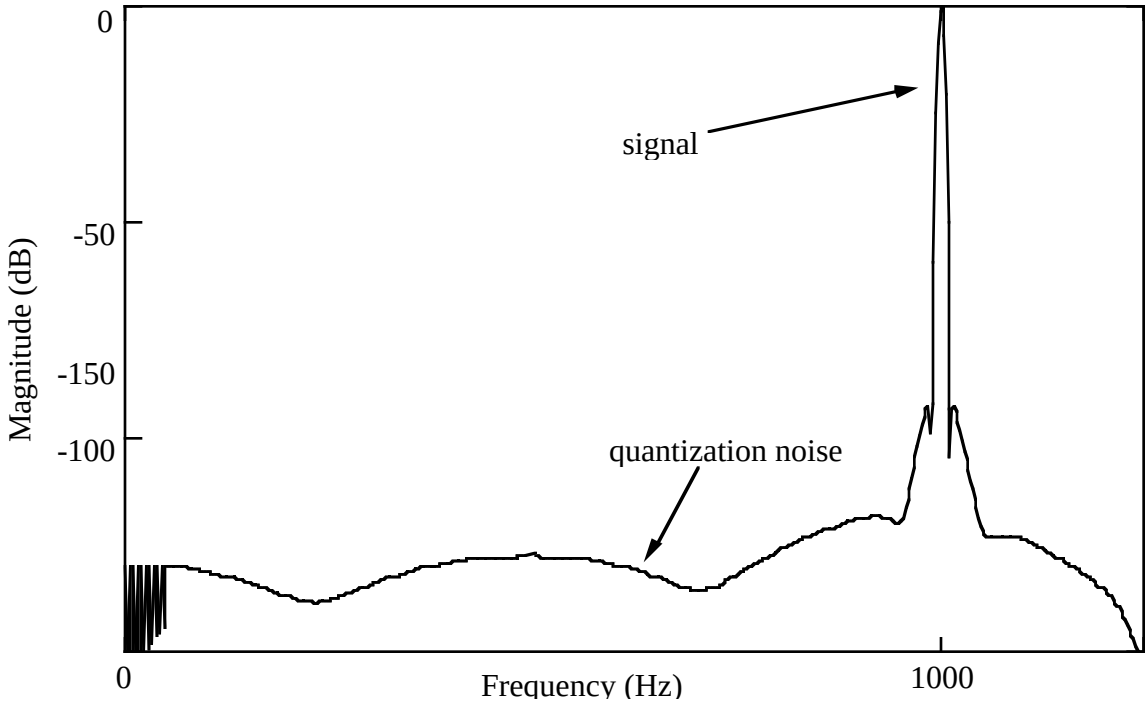
Digital Lowpass Filter



FIR or IIR digital low pass filter



After Digital Low Pass Filtering



Bit resolution

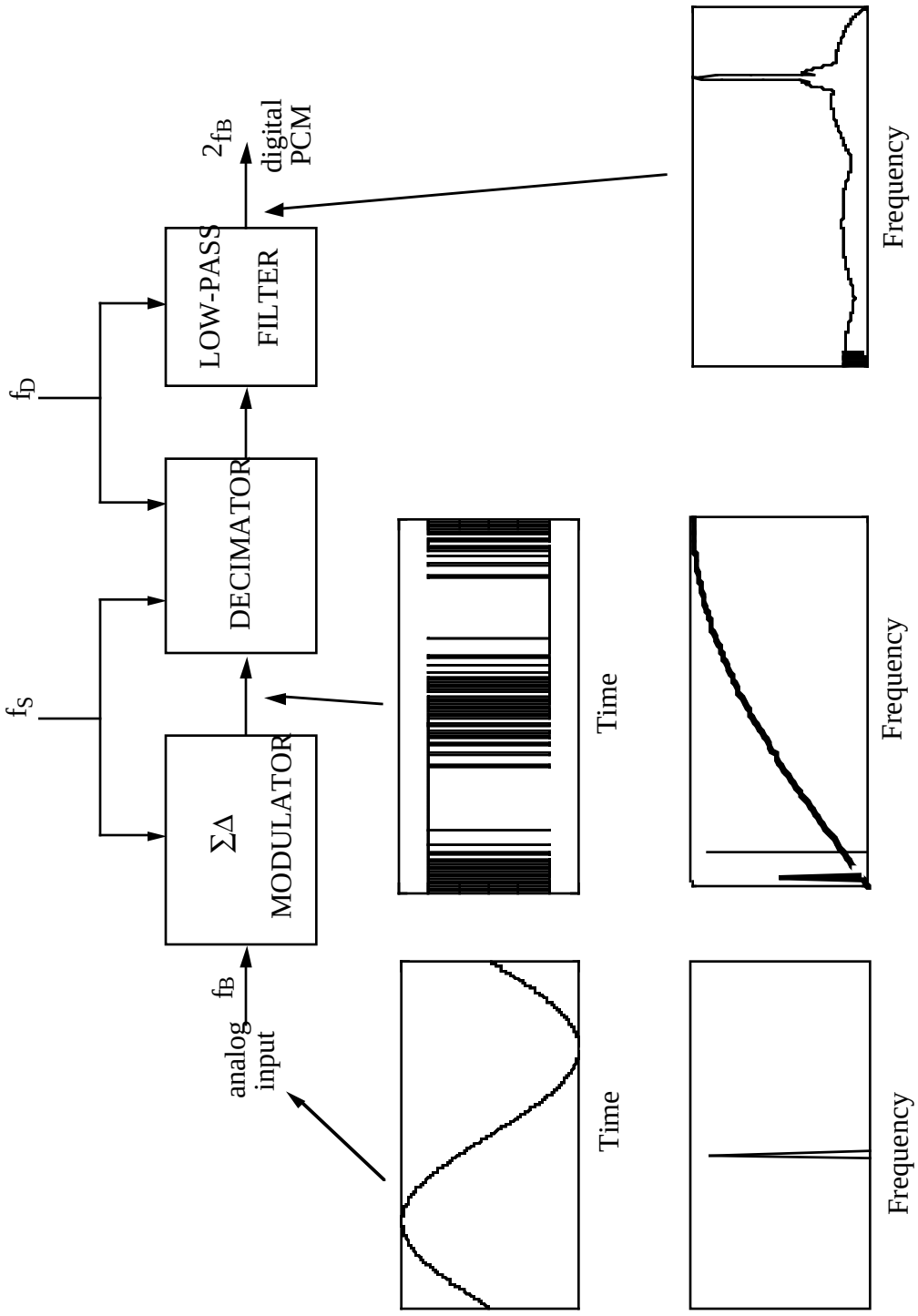
From the frequency response of above diagram, the signal-to-noise ratio (SNR)

$$SNR = 10\log_{10} \frac{\text{signal}}{\sum_{f=0}^{f_B} \text{noise}(f)} \quad \text{(dB)}$$

and

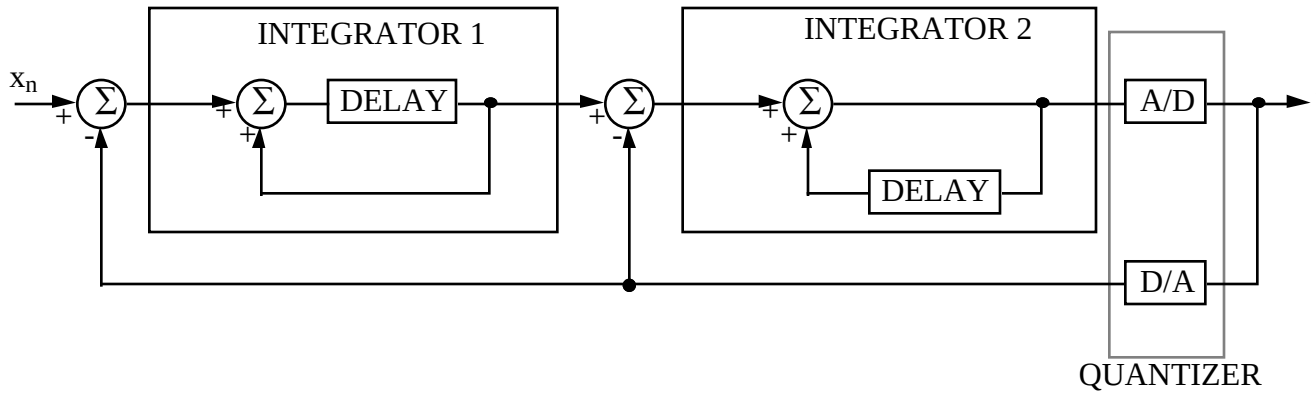
$$\text{Bit resolution (B)} \approx \frac{SNR(db)}{6dB}$$

System block in time domain and frequency domain



Second-Order ∑Δ Modulator

Second order ∑Δ modulator can be implemented by cascading two first order ∑Δ modulators.

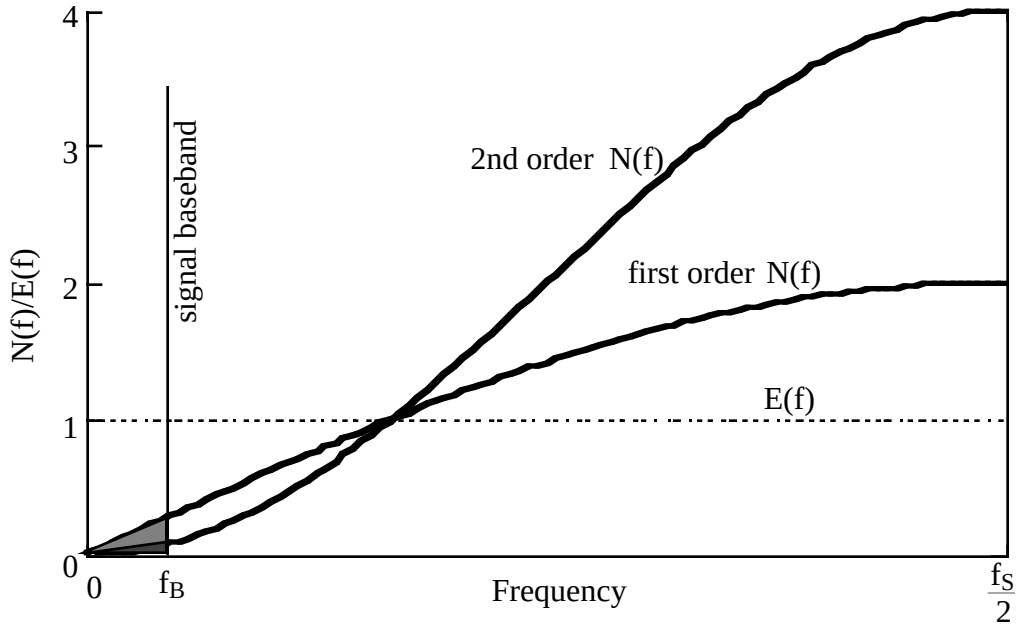


$$y_n = x_{n-1} + (e_n - 2e_{n-1} + e_{n-2})$$

The output of a second order ∑Δ modualtor y_n is the input signal delayed by one clock cycle x_{n-1}, plus the quantization noise difference $e_n - 2e_{n-1} + e_{n-2}$. The modulation noise spectrum density of $e_n - 2e_{n-1} + e_{n-2}$ is

$$N(f) = E(f)\left|1 - z^{-1}\right|^2 = E(f)\left|1 - e^{-j\omega\tau}\right|^2 = 4E(f)\sin^2\left(\frac{\omega\tau}{2}\right)$$

Noise Spectrum



Second-Order ∑Δ Modulator- Cond'd

The noise power in the signal band is

$$n_o = e_{rms}\frac{\pi^2}{\sqrt{5}}\ M^{-5/2} = \sqrt{\frac{\Delta^2}{12}}\frac{\pi^2}{\sqrt{5}}\ M^{-5/2} = \frac{\Delta\pi}{2\sqrt{15}}(M)^{-5/2},\ f_s >> f_o$$

Each doubling of the oversampling ratio reduces the modulation noise by 15 dB and increase the resolution by 2.5 bits.

Higher-Order Σ−Δ Modulators

Let L = the number of loops. The spectral density of the modulation can be written as

$$|N_L(f)| = e_{rms}\sqrt{2\tau}\left[2\sin\left(\frac{\omega\tau}{2}\right)\right]^L$$

The rms noise in the signal band is given approximately by

$$n_o \approx e_{rms}\frac{\pi^L}{\sqrt{2L+1}}(2f_B\tau)^{L+0.5}$$

This noise falls 3(2L+1) dB for every doubling of the sampling rate providing L+0.5 extra bits.

Decimation Filter

A filter function of $\left[\frac{\text{sinc}(\pi fN\tau)}{\text{sinc}(\pi f\tau)}\right]^{L+1}$ is close to being optimum for decimating the signal from an Lth-order Δ–Σ modulator.

Stability

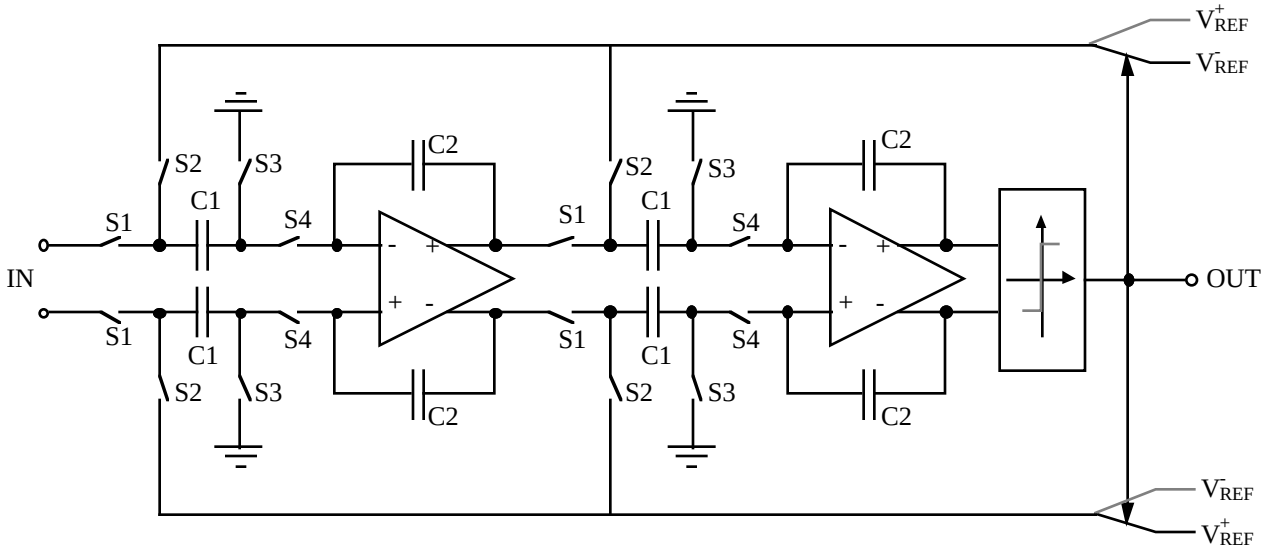
For orders greater than 2, the loop can become unstable. Loop configuration must be used that provide stability for order greater than two.

The modulation noise spectral density of a second-order, 1-bit $\Delta\Sigma$ modulator is given as

$$|N(f)| = \frac{4\Delta}{\sqrt{12}}\sqrt{\frac{2}{fs}}\ \sin^2\left(\frac{\omega t}{4}\right)$$

where Δ is the signal level out of the 1-bit quantizer and $f_S = (1/\tau)$ = the sampling frequency and is 10MHz. Find the signal bandwidth, fB, in Hz if the modulator is to be used in an 18 bit oversampled ADC. Be sure to state any assumption you use in working this problem.

Circuit Implementation of A Second Order ∑Δ Modulator



Fully differential, switched-capacitor integrators can reduce charge injection effect.

Circuit Tolerance of a Second Order ∑Δ Modulator

1. 20% variation of C1/C2 has only a minor impact on performance.
2. The Op Amp gain should be comparable to the oversampling ratio.
3. The unity-gain bandwidth of Op Amp should be at least an order of magnitude greater than the sampling rate.

SOURCES OF ERRORS IN ΣΔ A/D CONVERTERS

1. Quantization in time and amplitude

   Jitter and hysteresis

2. Linear Errors

   Gain and delay

3. Nonlinear Errors

   Harmonic distortion
   Thermal noise

Comparison of the Various Examples Discussed

Type of Converter	No. of Cycles/ Conver-sion	No. of Compar ators	Dependent on Passive Components	Resolu-tion	Speed	INL/DNL (LSB's)	Area	Power (mW)
Flash	1	2^{N-1}	Yes	Low	High	N/A	Largest	Largest
Two-Step Flash	2	31	Yes	10 bits	5Ms/s	±3/±0.6	54k $mils^2$	350
Pipeline	1 after initial delay	3	Yes	13 bits	250ks/s	±1.5/±0.5	3600 $mils^2$	15
Oversampl-ing	64	3	Yes	16 bits	24kHz	91dB	75.3k $mils^2$	110

X.11 -FUNDAMENTAL LIMITS OF SAMPLING A/D CONVERTERS

kT/C Noise

Assume that the ON resistance of a switch is R and the sampling capacitor is C and that the time to charge the capacitor fully is

$$T = \frac{1}{f_c} \approx 10RC \tag{1}$$

Set the value of the LSB $\left(= \frac{V_{ref}}{2^N}\right)$ equal to kT/C noise of the switch,

$$\frac{V_{ref}}{2^N} = \sqrt{\frac{kT}{C}} \tag{2}$$

Solve for C of (1) and substitute into (2) to get

$$\left(\frac{V_{ref}}{2^N}\right)^2 = 10kTRf_c \Rightarrow \quad 2^N\sqrt{f_c} = \frac{V_{ref}}{\sqrt{10kRT}} \tag{3}$$

Taking the log of both sides of (3) gives

$$N = -1.67 \log(f_c) + 3.3 \log(V_{ref}) - 1.67 \log(10kRT)$$

or

$$\boxed{N = 32.2 + 3.33 \log(V_{ref}) - 1.67 \log(Rf_c)}$$

(At room temperature)

kT/C Noise

Comparison of high-performance, monolithic A/D converters in terms of resolution versus sampling frequency with fundamental limits due to kT/C noise superimposed.

Fundamental Limits of Sampling A/D Converters - Continued

Maximum Sample Rate

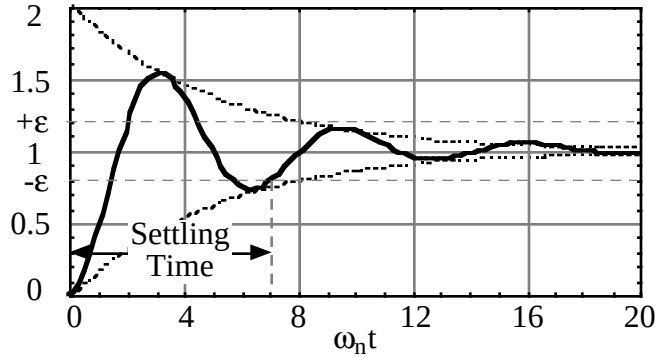
Assume that the maximum sample rate is determined by the time required for the amplifiers and/or sample-hold circuits to settle with the desired accuracy for high resolution. Further assume that the dynamics of these circuits can be modeled by a second-order system with a transfer function of

$$\frac{A(s)}{A(0)} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

If $\omega_n \approx$ GB of the circuit and if the system is underdamped, then the step response is given as

$$\frac{v_o(t)}{A(0)} = 1 - \left[\frac{e^{-\zeta GBt}}{\sqrt{1-\zeta^2}}\right] \sin\left(\sqrt{1-\zeta^2}\ GB \cdot t + \phi\right)$$

This response looks like the following,



If we define the error ($\pm\varepsilon$) in v_o settling to A(0) as the multiplier of the sinusoid, then an expression for the settling time can be derived as

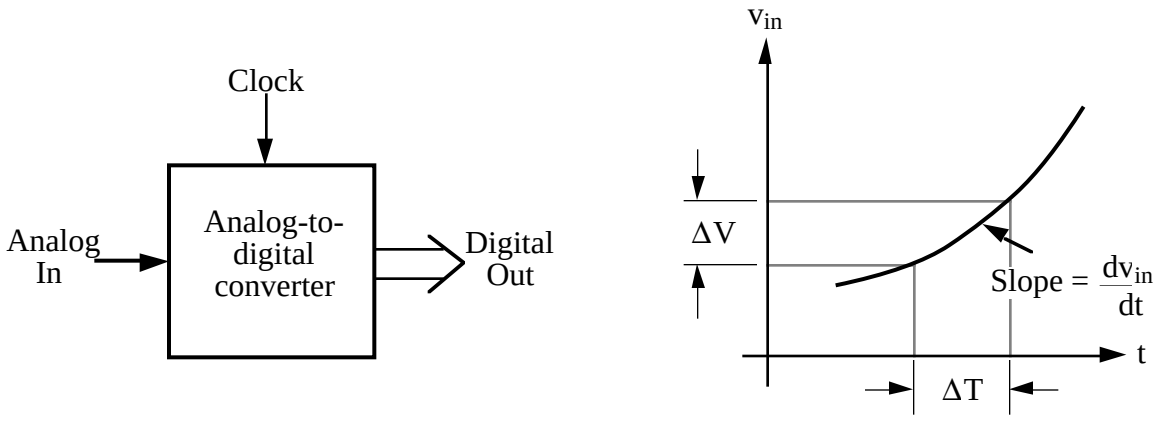
$$t_s = \frac{1}{2\pi\zeta GB} \ln\left(\frac{e^{-\zeta GBt}}{\sqrt{1 - \zeta^2}}\right) \Rightarrow f_{sample} = \frac{1}{t_s} = \frac{2\pi\zeta GB}{\ln\left(\frac{1}{\varepsilon\sqrt{1-\zeta^2}}\right)}$$

For reasonable values of ζ, f_{sample} can be approximated as

$$\boxed{f_{sample} \approx \frac{\pi GB}{10} = \frac{GB}{3}}$$

Aperature Uncertainty (Jitter)

A problem in all clocked or sampled A/D converters.



$$\Delta V = \text{slope} \times \Delta T = \frac{dv_{in}}{dt}\ \Delta T$$

$$\Delta T = \text{Aperature uncertainty} = \frac{\Delta V}{\frac{dV_{in}}{dt}} = \frac{V_{ref}/2^N}{dv_{in}/dt}$$

Assume that $v_{in}(t) = V_p \sin \omega t$

$$\left|\frac{dv_{in}}{dt}\right|_{max} = \omega V_p$$

$$\Delta T = \frac{V_{ref}}{2^N} \times \frac{1}{\omega V_p} \approx \frac{V_{ref}}{2^N \omega V_{ref}} = \frac{1}{2^N \omega}$$

Therefore, $\Delta T = \frac{1}{2\pi f 2^N} = \frac{1}{\pi f 2^{N+1}}$

Suppose f = 100kHz and N = 8, $\Delta T = \frac{1}{200\pi K x 2^9} = 6.22\text{ns}$

Clock accuracy = $\frac{6.22\text{ns}}{10{,}000\text{ns}} = 0.06\% = \frac{622\text{ppm}}{?}$

X.12 - SUMMARY OF A/D CONVERTERS

Typical Performance Characteristics

A/D Architecture	Typical Performance Characteristics
Serial $\frac{1}{f_c} = 2^N T$	1-100 conversions/sec., 12-14 bit accuracy, requires no element-matching, a stable voltage reference is necessary
Successive Approximation $\frac{1}{f_c} \approx NT$	10,000-100,000 conversions/sec., 8-10 bits of untrimmed or uncalibrated accuracy, 12-14 bits of trimmed or calibrated accuracy
High Speed $T < \frac{1}{f_c} < NT$	1 to 40 megaconversions/sec., 7-9 bits of accuracy, 10-12 bits of accuracy with error correction and other techniques
Oversampling $\frac{1}{f_c} << T$	8,000-600,000 conversions/sec., 12-16 bits accuracy, requires linear integrators but no precision passive components, minimizes noise and offsets

Conclusions

- The best A/D converter depends upon the application
- Both resolution and speed are ultimately limited by the accuracy of the process
- High resolution A/D's will be more oriented toward "signal averaging" type converters, particularly with shorter channel lengths